Low Power & High-Resolution Audio Processing System SoC for Portable Sound Solution

ON Semiconductor®

www.onsemi.com

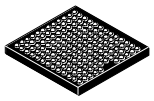
LC823455

Description

LC823455 is an audio processing System−on−Chip (SoC) for recording and playback, with High−Resolution 32−bit & 192 kHz audio processing capability that provides the key functions required for portable audio solutions.

It has a Dual CPU configuration and a DSP providing intensive processing capability, 4316 KB of internal SRAM that supports the implementation of large-scale programs for WLAN applications, and multiple interfaces for increased extensibility. Its features an extensive range of functions including SBC/AAC codec and Active Noise Canceller by the DSP, UART and ASRC − applicable for wearable audio applications. The highly integrated implementation of this rich set of analog functions results in a miniature footprint with ultra− low power consumption. This, along with its high performance, makes the LC823455 suitable for portable audio markets such as Wireless headsets.

This document describes features, basic functions, electrical specifications, characteristics, application diagrams and package dimension of this SoC.



WLCSP120, 4.086x4.086x0.62
CASE 567WG

ORDERING INFORMATION

See detailed ordering and shipping information on page 106 of this data sheet.

Features

- Ultra Low Power Consumption
- Arm® Cortex®−M3 Dual Core
- Proprietary 32−bit DSP Core (LPDSP32)
- Internal Large−Scale Size SRAM : 4316 KB (4MB + 220 KB)
- High−Resolution 32−bit & 192 kHz Audio Processing Capability
- Several DSP Codes Available for Audio Functions
- Hard−Wired Audio Functions Built−In:
  MP3 decoder, MP3 encoder,
  6 band Equalizer
  Synchronous SRC, Asynchronous SRC, etc.
- Analog Blocks Built−in:
  System PLL, Audio PLL,
  16−bit DAC, Class−D amp, etc.
- USB2.0 Device with an Integrated PHY
  eMMC and SD Card I/F,
  Serial Flash I/F(Quad) with Cache Memory,
  SPI, UART, I2C, etc.

Typical Applications

- Wearable Earbuds
- Wearable Headphone
- Wireless Speaker
- IC Recorder

Table of Contents

ABSTRACT

Features

- Cortex−M3 Dual Core, AMBA® (AHB/APB) system
  - Internal SRAM (4 M-byte)
  - Internal ROM (256 k-byte). Boot code, Standard Functions
  - SDRAM Controller (1 * CS)
    64M to 256Mbit SDRAM / Mobile SDRAM
  - External Memory Controller (2 * CS) NOR FLASH, SRAM, ROM supported, 8/16 bit I/F LCD controller supported
    Internal ROM boot and External memory device boot available
  - DMA Controller (8 ch)
  - Interrupt Controller (External 90 ch, Internal 83 ch)
  - SPI (2 ch)
  - Pseudo SRAM I/F (1 ch)
  - Serial Flash I/F (1 ch)
  - Quad SPI, cache memory (16 k-byte, 4way set associative, 128 line) function available
  - UART (3ch)
    UART1, UART2: w/flow control (CTS, RTS)
    UART0: w/o flow control
  - I2C (2ch) Single Master, Full/Standard
  - GPIO (90 ch)
  - Pin multiplex function (I2C:2 ch, SPI:2 ch, UART:3 ch, MTM:2 ch, DMIC:2 ch x 2)
  - Plain Timer w/ Watch Dog Timer (1 ch×3)
  - Multiple Timer (2 ch×4)
  - 12 bit ADC (8 ch)
  - SD Card I/F (3 ch)
    eSD/eMMC, UHS−I, w/o CPRM
    - SD0: eSD/eMMC boot supported (Internal ROM Boot function)
    - SD1: 1.8 V/3.3 V dedicated power supply
    - SD2 :
  - USB2.0 Device (HS/FS) Controller. Integrated PHY
    Xtal (XT1) is required for USB function. 12, 19.2, 24 MHz for device
    w/o OTG function. Host and Device share an integrated PHY.
  - Real Time Clock
    2 modes below are available
    - General RTC mode : RTC w/o key input
    - KeyInt RTC mode : RTC w/ key input which enables power on function
  - SWD (Serial Wire Debug) is supported as the debug interface
    SWV (Serial Wire Viewer) is supported as the trace interfaceOnly one of Cortex−M3 Dual Core can be traced

Availability of features explained here depends on products.

- MP3 hard wired encoder/decoder
  - MP3 MPEG1, MPEG2, MPEG2.5
    - Sampling rate: 8 kHz,11.025 kHz,12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kH
    - Bit rate: 8 Kbps to 320 Kbps (Decoder−VBR supported)
- LPDSP32 system
  - Internal SRAM (220 kbyte)
  - Audio codec
    - MP3
    - WMA
    - AAC
    - SBC
    - FLAC, etc.
  - Audio function
    - Active Noise Canceller
    - 1−mic/2−mic Noise Canceller for Recorder
    - 2−mic Noise Caneceller for Hands Free
    - Echo Canceller
    - Variable Speed Control playback etc.
  - JTAG ICE

[1] MPEG Layer−3 audio coding technology licensed from Fraunhofer IIS and Thomson. Supply of this product does not convey license nor imply any right to distribute content created with this product in revenue−generating broadcast systems (terrestrial, satellite, cable and/or other distribution channels), streaming applications (via Internet, intranets and/or networks), other content distribution systems (pay−audio or audio−on−demand applications and the like) or on physical media (compact discs, digital versatile discs, semiconductor chips, hard drives, memory cards and the like). For details, please visit http://mp3licensing.com/
Supply of this product does not convey license under the relevant intellectual property of Thomson and/or Fraunhofer Gesellschaft nor imply any right to use this product in any finished end user or ready−to−use final product. An independent license for such use is required. For details, please visit http://mp3licensing.com/

[2] This product contain technology of Microsoft company ownership, and you cannot distribute or use without getting license from Microsoft Licensing Company.

- Bluetooth Protocol Stack available
- Audio
  - MP3 hard wired encoder/decoder, MP3 MPEG1, MPEG2, MPEG2.5
    - Sampling rate: 8 kHz,11.025 kHz,12 kHz,16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48kHz
    - Bit rate :8 Kbps to 320 Kbps (Decoder−VBR supported)
  - Other audio functions available
    - 6 band Equalizer (EQ3)
    - Hardware Mixer
    - Volume, Mute
    - Level Meter
    - Audio Timer w/ interrupt generation
    - 16/24/32 bit 192 kHz PCM I/F (2ch×2). Master/slave, I2S
    - SSRC (Synchronous Sampling Rate Converter) 0.25 to 64 conversion capable
    - ASRC (Asynchronous Sampling Rate Converter) Jitter reducing function supporting USB audio class and Bluetooth streaming
    - Beep generator
    - Digital Microphone I/F (2ch x2), Sampling rate : up to 48 kHz, Support up to 4 PDM Digital Microphones
    - 16 bit Audio DAC (2 ch) w/ Class−D Amplifier for Head Phone (2 ch). Requires external LC LPF
- Audio clock generation
  - Dedicated PLL for audio
  - Selectable PLL reference clock
    XT1 (12, 19.2, 24 MHz Main xtal)
    XTRTC (32.768 kHz RTC xtal)
    PCM I/F MCLK0 (/MCLK1), BCK0, BCK1
- Power supply
  - Typical voltage
    - LOGIC(Vdd1),XT1(VddXT1), PLL1(AVddPLL1), PLL2(AVddPLL2) = 1.0 V
    - RTC(VddRTC) = 1.0 V
    - I/O(Vdd2) = 1.8 V or 3.3 V
    - SD1(VddSD1) = 1.8 V or 3.3 V
    - ADC(AVddADC) = 1.8V
    - USB PHY(DVddUSBPHY1) = 1.0 V, (AVddUSBPHY2) = 3.3 V, (AVddUSBPHY18) = 1.8 V
    - Class−D Amplifier (AVddDAMPL,AVddDAMPR) = 1.5 V

[3] The product name for which Bluetooth Protocol Stack is available is determined. Please contact our representative for license fee for the Stack.

Package Codes and Functional Differences

Table 1. FUNCTIONAL DIFFERENCES

Function	Package Code	
	XA	**TBD**
Package	**WLP120**	**TBD (240pin)**
SDRAM Controller	–	Available
External Memory Controller	–	Available
SD0	Shared pins with S−Flash function	Dedicated
P−SRAM	–	Available
12 bit ADC	3ch	8ch
PLL1 PLL2	Only Internal Loop Filter	Internal / ExternalLoop Filter
XTALINFO[1:0] input	“00” (24 MHz)	Available
RTCMODE input	“0” (KEYINT RTC mode)	Available
BACKUPB input	Connected with VDET internally	Available
KEYINT input	2ch	3ch
External Interrupt	52 ch	90 ch
GPIO	52 ch	90 ch

Block Diagram

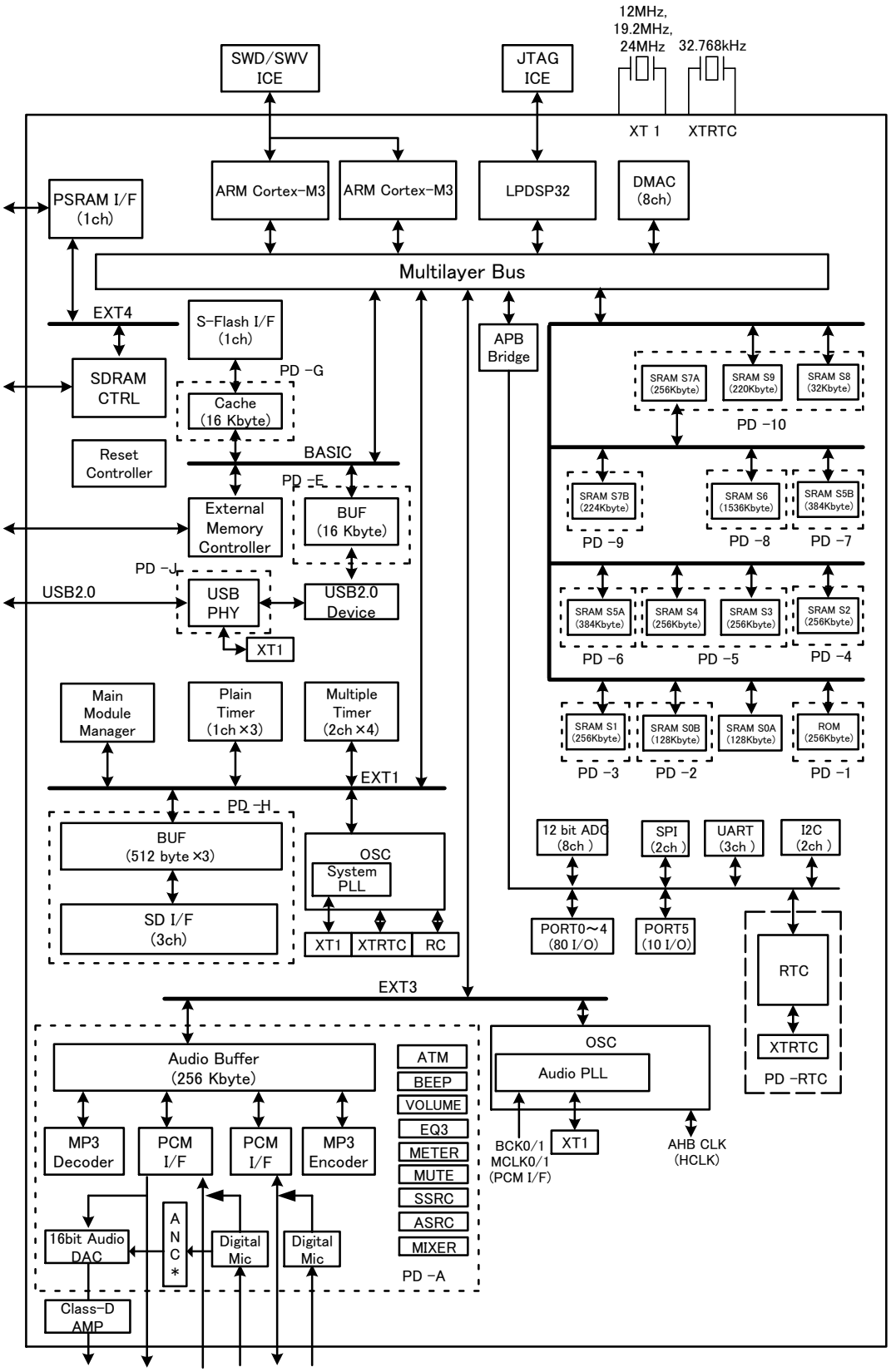


Figure 1. Top

Bus Matrix

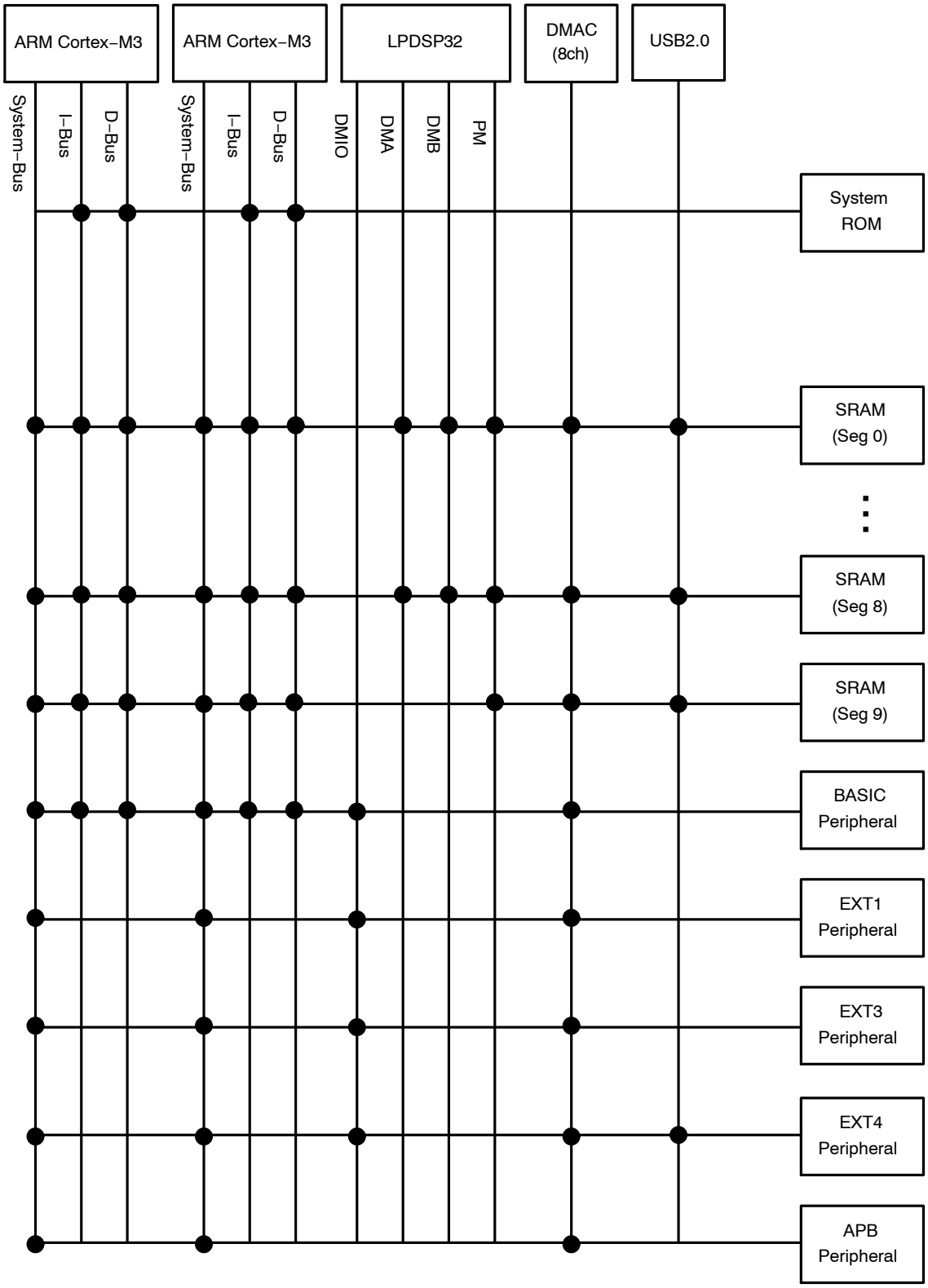


Figure 2. Bus Matrix

Audio

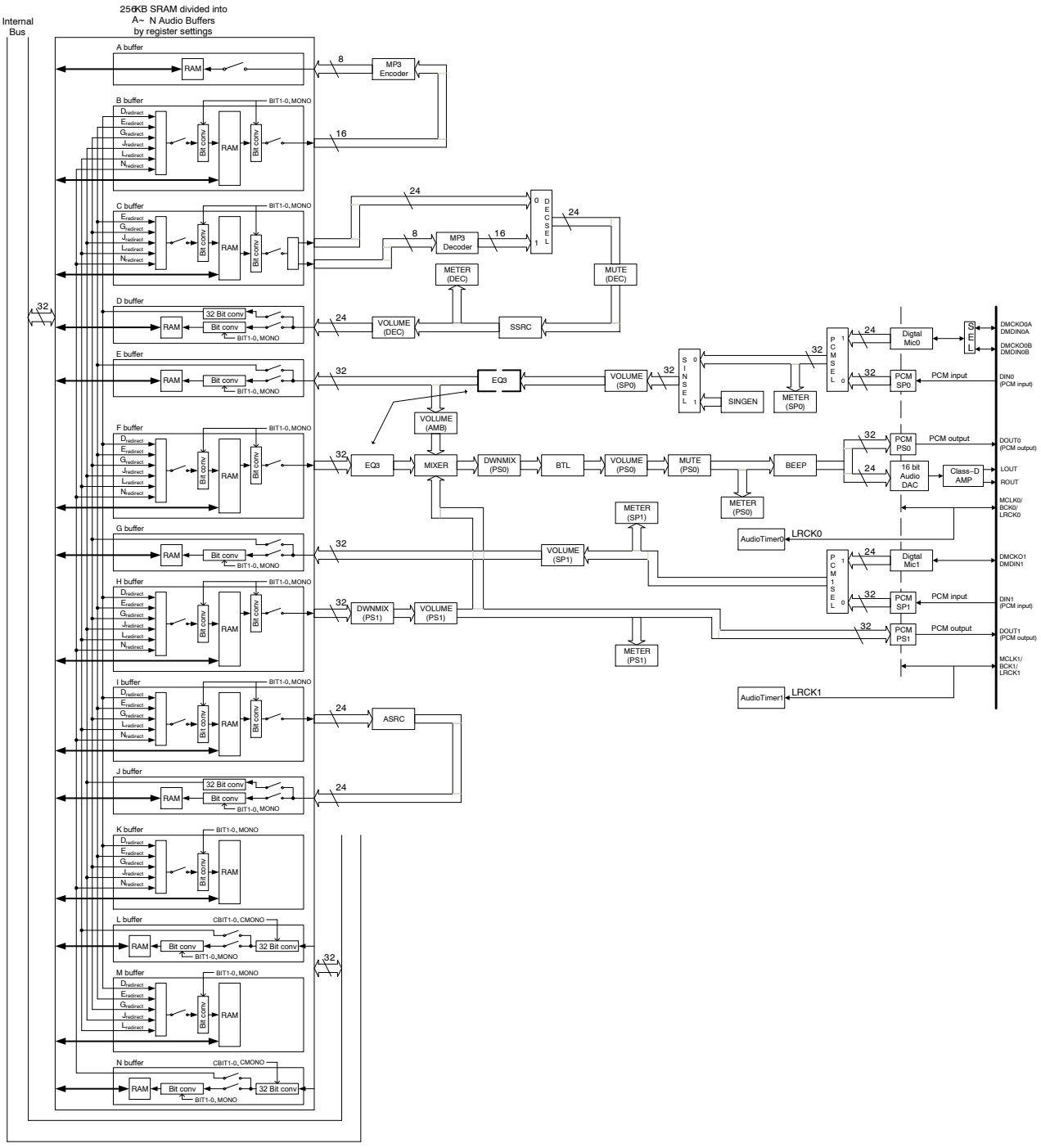


Figure 3. Audio

Clock Hierarchy

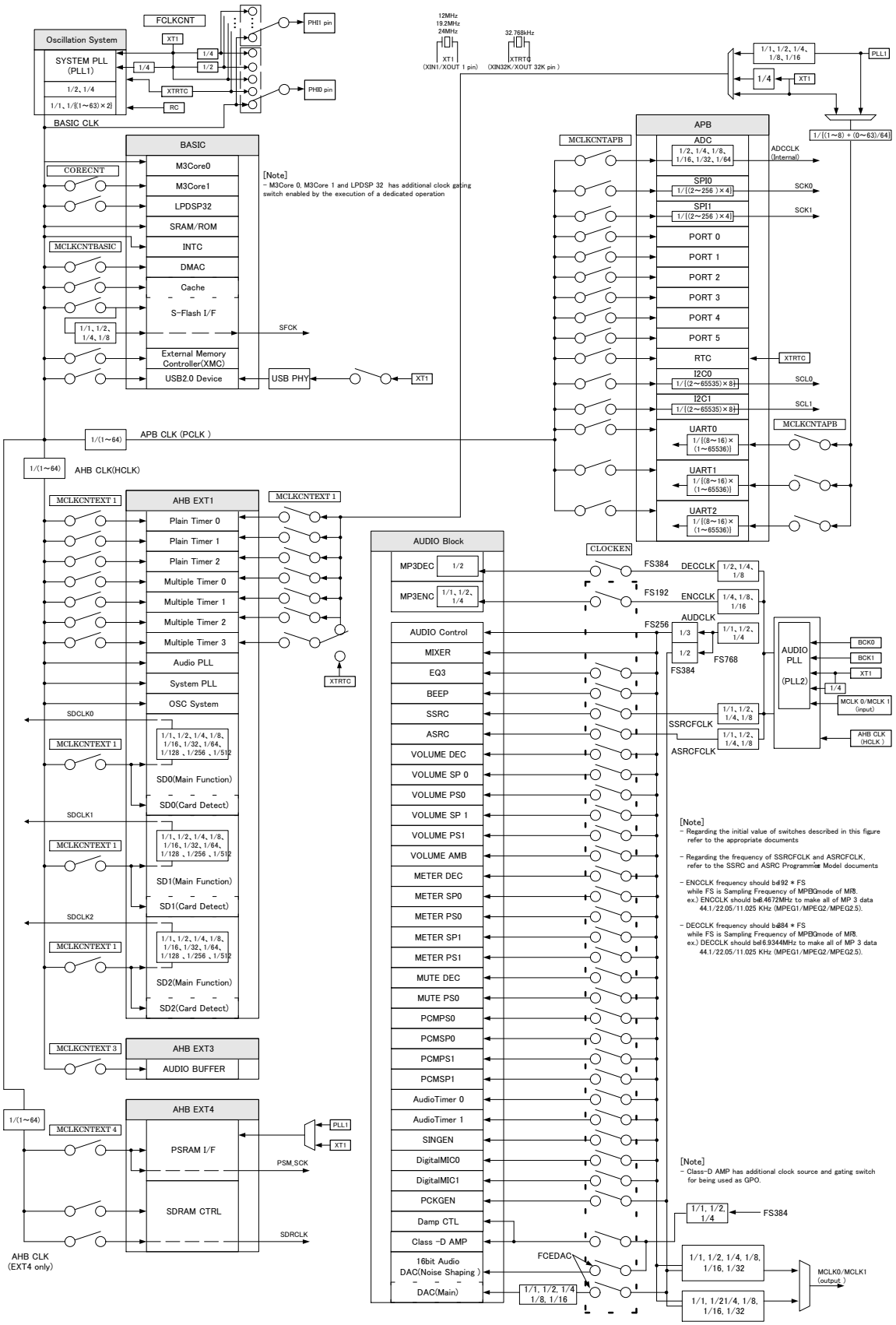


Figure 4. Clock Hierarchy

Memory Map

All Areas (Cortex−M3)

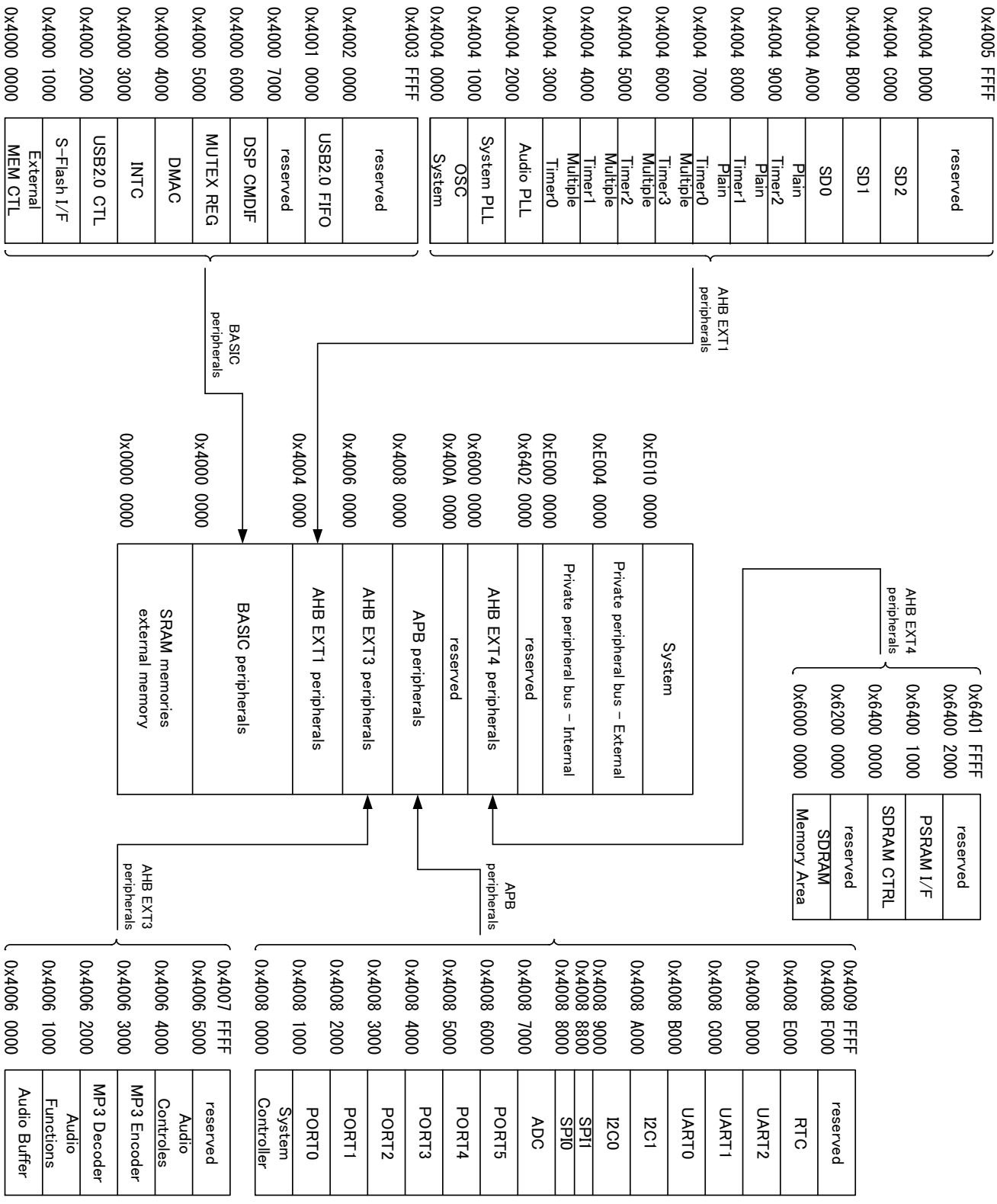


Figure 5. All Areas (Cortex−M3)

Code Area (Cortex−M3)

Table 2. CODE AREA (CORTEX−M3) − UNREMAPPED (AFTER RESET)

Address	Master / Slave		Cortex−M3−0			Cortex−M3−1			DMAC	USB20
			System−Bus	I−Bus	D−Bus	System−Bus	I−Bus	D−Bus		
0x1C00 0000	Reserved									
0x1A00 0000	External memory 1			○			○			
0x1800 0000	External memory 0			○			○			
0x0600 0000	Reserved									
0x0500 0000	S−Flash I/F (Memory, Cache)			○			○			
0x0254 0000	Reserved									
0x0250 0000	256 KB Internal ROM			○			○			
0x0243 7000	Reserved									
0x0240 0000	220 KB Internal SRAM (seg 9)			○			○			
0x023F 8000	32 KB Internal SRAM (seg 8)			○			○			
0x023C 0000	480 KB Internal SRAM (seg 7)	224 KB (seg 7−B)		○			○			
0x0238 0000		256KB (seg 7−A)		○			○			
0x0220 0000	1536 KB Internal SRAM (seg 6)			○			○			
0x021A 0000	768 KB Internal SRAM (seg 5)	384 KB (seg 5−B)		○			○			
0x0214 0000		384 KB (seg 5−A)		○			○			
0x0210 0000	256 KB Internal SRAM (seg 4)			○			○			
0x020C 0000	256 KB Internal SRAM (seg 3)			○			○			
0x0208 0000	256 KB Internal SRAM (seg 2)			○			○			
0x0204 0000	256 KB Internal SRAM (seg 1)			○			○			
0x0202 0000	256 KB Internal SRAM (seg 0)	128 KB (seg 0−B)		○			○			
0x0200 0000		128 KB (seg 0−A)		○			○			
0x0004 0000	Reserved									
0x0000 0000	256 KB Internal ROM Shadow Area			○			○			

Table 3. CODE AREA (CORTEX−M3) − REMAPPED (REMAP[1:0]=2'B01)

Address	Master / Slave		Cortex−M3−0			Cortex−M3−1			DMAC	USB20
			System−Bus	I−Bus	D−Bus	System−Bus	I−Bus	D−Bus		
0x1C00 0000	Reserved									
0x1A00 0000	External memory 1			○			○			
0x1800 0000	External memory 0			○			○			
0x0600 0000	Reserved									
0x0500 0000	S−Flash I/F (Memory, Cache)			○			○			
0x0254 0000	Reserved									
0x0250 0000	256 KB Internal ROM			○			○			
0x0243 7000	Reserved									
0x0240 0000	220 KB Internal SRAM (seg 9)			○			○			
0x023F 8000	32 KB Internal SRAM (seg 8)			○			○			
0x023C 0000	480 KB Internal SRAM (seg 7)	224 KB (seg 7−B)		○			○			
0x0238 0000		256 KB (seg 7−A)		○			○			
0x0220 0000	1536 KB Internal SRAM (seg 6)			○			○			
0x021A 0000	768 KB Internal SRAM (seg 5)	384 KB (seg 5−B)		○			○			
0x0214 0000		384 KB (seg 5−A)		○			○			
0x0210 0000	256 KB Internal SRAM (seg 4)			○			○			
0x020C 0000	256 KB Internal SRAM (seg 3)			○			○			
0x0208 0000	256 KB Internal SRAM (seg 2)			○			○			
0x0204 0000	256 KB Internal SRAM (seg 1)			○			○			
0x0202 0000	256 KB Internal SRAM (seg 0)	128 KB (seg 0−B)		○			○			
0x0200 0000		128 KB (seg 0−A)		○			○			
0x0004 0000	Reserved									
0x0002 0000	256 KB Internal SRAM (seg 0) Shadow Area	128 KB (seg 0−B)		○			○			
0x0000 0000		128 KB (seg 0−A)		○			○			

Table 4. CODE AREA (CORTEX−M3) − REMAPPED (REMAP[1:0]=2'B11)

Address	Master / Slave		Cortex−M3−0			Cortex−M3−1			DMAC	USB20
			System−Bus	I−Bus	D−Bus	System−Bus	I−Bus	D−Bus		
0x1C00 0000	Reserved									
0x1A00 0000	External memory 1			○			○			
0x1800 0000	External memory 0			○			○			
0x0600 0000	Reserved									
0x0500 0000	S−Flash I/F (Memory, Cache)			○			○			
0x0254 0000	Reserved									
0x0250 0000	256 KB Internal ROM			○			○			
0x0243 7000	Reserved									
0x0240 0000	220 KB Internal SRAM (seg 9)			○			○			
0x023F 8000	32 KB Internal SRAM (seg 8)			○			○			
0x023C 0000	480 KB Internal SRAM (seg 7)	224 KB (seg 7−B)		○			○			
0x0238 0000		256 KB (seg 7−A)		○			○			
0x0220 0000	1536KB Internal SRAM (seg 6)			○			○			
0x021A 0000	768 KB Internal SRAM (seg 5)	384 KB (seg 5−B)		○			○			
0x0214 0000		384 KB (seg 5−A)		○			○			
0x0210 0000	256KB Internal SRAM (seg 4)			○			○			
0x020C 0000	256KB Internal SRAM (seg 3)			○			○			
0x0208 0000	256KB Internal SRAM (seg 2)			○			○			
0x0204 0000	256KB Internal SRAM (seg 1)			○			○			
0x0202 0000	256 KB Internal SRAM (seg 0)	128 KB (seg 0−B)		○			○			
0x0200 0000		128 KB (seg 0−A)		○			○			
0x0000 0000	External memory 0 Shadow Area			○			○			

SRAM Area (Cortex−M3)

Table 5. SRAM AREA (CORTEX−M3)

Address	Master / Slave		Cortex−M3−0			Cortex−M3−1			DMAC	USB20
			System−Bus	I−Bus	D−Bus	System−Bus	I−Bus	D−Bus		
0x2600 0000	Reserved									
0x2500 0000	S−Flash I/F (Memory, Cache)		○			○			○	
0x2400 0000	S−Flash I/F (Memory, No Cache)		○			○			○	
0x2043 7000	Reserved									
0x2040 0000	220 KB Internal SRAM (seg 9) Shadow area		○			○			○	
0x203F 8000	32 KB Internal SRAM (seg 8) Shadow area		○			○			○	
0x203C 0000	480 KB Internal SRAM (seg 7) Shadow area	224 KB (seg 7−B)	○			○			○	
0x2038 0000		256 KB (seg 7−A)	○			○			○	
0x2020 0000	1536 KB Internal SRAM (seg 6) Shadow area		○			○			○	
0x201A 0000	768 KB Internal SRAM (seg 5) Shadow area	384 KB (seg 5−B)	○			○			○	
0x2014 0000		384 KB (seg 5−A)	○			○			○	
0x2010 0000	256 KB Internal SRAM (seg 4) Shadow area		○			○			○	
0x200C 0000	256 KB Internal SRAM (seg 3) Shadow area		○			○			○	
0x2008 0000	256 KB Internal SRAM (seg 2) Shadow area		○			○			○	
0x2004 0000	256 KB Internal SRAM (seg 1) Shadow area		○			○			○	
0x2002 0000	256 KB Internal SRAM (seg 0) Shadow area	128 KB (seg 0−B)	○			○			○	
0x2000 0000		128 KB (seg 0−A)	○			○			○	

Other Areas (Cortex−M3)

Table 6. OTHER AREAs (CORTEX−M3)

Address	Master / Slave	Cortex−M3−0			Cortex−M3−1			DMAC	USB20
		System−Bus	I−Bus	D−Bus	System−Bus	I−Bus	D−Bus		
0xE010 0000	Reserved								
0xE00F F000	ROM table	○ (Note 1)			○ (Note 1)				
0xE00F E000	CORE REG	○ (Note 1)			○ (Note 1)				
0xE004 1000	Reserved								
0xE004 0000	TPIU	○ (Note 1)			○ (Note 1)				
0xE000 F000	Reserved								
0xE000 E000	NVIC	○ (Note 1)			○ (Note 1)				
0xE000 3000	Reserved								
0xE000 2000	FPB	○ (Note 1)			○ (Note 1)				
0xE000 1000	DWT	○ (Note 1)			○ (Note 1)				
0xE000 0000	ITM	○ (Note 1)			○ (Note 1)				
0x6400 2000	Reserved								
0x6400 1000	PSRAM I/F	○			○			○	
0x6400 0000	SDRAM CTRL	○			○				
0x6200 0000	Reserved								
0x6000 0000	SDRAM Memory area	○			○			○	
0x4008 F000	Reserved								
0x4008 E000	RTC	○			○				
0x4008 D000	UART2	○			○			○	
0x4008 C000	UART1	○			○			○	
0x4008 B000	UART0	○			○			○	
0x4008 A000	I2C1	○			○				
0x4008 9000	I2C0	○			○				
0x4008 8800	SPI1	○			○			○	
0x4008 8000	SPI0	○			○			○	
0x4008 7000	ADC	○			○			○	

Table 6. OTHER AREAs (CORTEX−M3) (continued)

Address	Master / Slave	Cortex−M3−0			Cortex−M3−1			DMAC	USB20
		System−Bus	I−Bus	D−Bus	System−Bus	I−Bus	D−Bus		
0x4008 6000	PORT5	○			○				
0x4008 5000	PORT4	○			○				
0x4008 4000	PORT3	○			○				
0x4008 3000	PORT2	○			○				
0x4008 2000	PORT1	○			○				
0x4008 1000	PORT0	○			○				
0x4008 0000	System Controller	○			○				
0x4006 5000	Reserved								
0x4006 4000	Audio Controls	○			○				
0x4006 3000	MP3 Encoder	○			○				
0x4006 2000	MP3 Decoder	○			○				
0x4006 1000	Audio Functions	○			○				
0x4006 0000	Audio Buffer	○			○			○	
0x4004 D000	Reserved								
0x4004 C000	SD2	○			○			○	
0x4004 B000	SD1	○			○			○	
0x4004 A000	SD0	○			○			○	
0x4004 9000	Plain Timer2	○			○				
0x4004 8000	Plain Timer1	○			○				
0x4004 7000	Plain Timer0	○			○				
0x4004 6000	Multiple Timer3	○			○				
0x4004 5000	Multiple Timer2	○			○				
0x4004 4000	Multiple Timer1	○			○				
0x4004 3000	Multiple Timer0	○			○				
0x4004 2000	Audio PLL	○			○				
0x4004 1000	System PLL	○			○				
0x4004 0000	OSC System	○			○				

Table 6. OTHER AREAs (CORTEX−M3) (continued)

Address	Master / Slave	Cortex−M3−0			Cortex−M3−1			DMAC	USB20
		System−Bus	I−Bus	D−Bus	System−Bus	I−Bus	D−Bus		
0x4002 0000	Reserved								
0x4001 0000	USB2.0 FIFO	○			○				
0x4000 7000	Reserved								
0x4000 6000	DSP CMDIF	○			○				
0x4000 5000	MUTEX REG	○			○				
0x4000 4000	DMAC	○			○				
0x4000 3000	INTC	○			○				
0x4000 2000	USB2.0 CTL	○			○				
0x4000 1000	S−Flash I/F	○			○				
0x4000 0000	External MEM CTL	○			○				

1. Access from internal peripheral bus(AHB/APB)

LPDSP32

Table 7. LPDSP32 – DMA

Address	Master / Slave		LPDSP32 DMA
0x40 0000	Reserved		
0x3F 8000	32 KB Internal SRAM (seg 8)		○
0x3C 0000	480 KB Internal SRAM (seg 7)	224 KB (seg 7−B)	○
0x38 0000		256 KB (seg 7−A)	○
0x20 0000	1536 KB Internal SRAM (seg 6)		○
0x1A 0000	768 KB Internal SRAM (seg 5)	384 KB (seg 5−B)	○
0x14 0000		384 KB (seg 5−A)	○
0x10 0000	256 KB Internal SRAM (seg 4)		○
0x0C 0000	256 KB Internal SRAM (seg 3)		○
0x08 0000	256 KB Internal SRAM (seg 2)		○
0x04 0000	256 KB Internal SRAM (seg 1)		○
0x02 0000	256 KB Internal SRAM (seg 0)	128 KB (seg 0−B)	○
0x00 0000		128 KB (seg 0−A)	○

Table 8. LPDSP32 – DMB

Address	Master / Slave		LPDSP32 DMB
0xC0 0000	Reserved		
0xBF 8000	32 KB Internal SRAM (seg 8)		○
0xBC 0000	480 KB Internal SRAM (seg 7)	224 KB (seg 7−B)	○
0xB8 0000		256 KB (seg 7−A)	○
0xA0 0000	1536 KB Internal SRAM (seg 6)		○
0x9A 0000	768 KB Internal SRAM (seg 5)	384 KB (seg 5−B)	○
0x94 0000		384 KB (seg 5−A)	○
0x90 0000	256 KB Internal SRAM (seg 4)		○
0x8C 0000	256 KB Internal SRAM (seg 3)		○
0x88 0000	256 KB Internal SRAM (seg 2)		○
0x84 0000	256 KB Internal SRAM (seg 1)		○
0x82 0000	256 KB Internal SRAM (seg 0)	128 KB (seg 0−B)	○
0x80 0000		128 KB (seg 0−A)	○

Table 9. LPDSP32 – DMIO

Address	Master / Slave	LPDSP32
		DMIO
0xF0 2000	Reserved	
0xF0 1000	PSRAM I/F	○
0xF0 0000	SDRAM CTRL	○
0xD0 0000	SDRAM Memory Area	○
0xC6 5000	Reserved	
0xC6 4000	Audio Controles	○
0xC6 3000	MP3 Encoder	○
0xC6 2000	MP3 Decoder	○
0xC6 1000	Audio Functions	○
0xC6 0000	Audio Buffer	○
0xC4 A000	Reserved	
0xC4 9000	Plain Timer2	○
0xC4 8000	Plain Timer1	○
0xC4 7000	Plain Timer0	○
0xC4 6000	Multiple Timer3	○
0xC4 5000	Multiple Timer2	○
0xC4 4000	Multiple Timer1	○
0xC4 3000	Multiple Timer0	○
0xC4 2000	Audio PLL	○
0xC4 1000	System PLL	○
0xC4 0000	OSC System	○
0xC0 7000	Reserved	
0xC0 6000	DSP CMDIF	○
0xC0 5000	MUTEX REG	○
0xC0 4000	DMAC	○
0xC0 3000	INTC	○
0xC0 0000	Reserved	

Table 10. LPDSP32 − PM

Address	Master / Slave		LPDSP32 PM
0x50 3332	Reserved		
0x50 0000	32 KB Internal SRAM (seg 8)		○
0x4B 0000	Reserved		
0x48 0000	480 KB Internal SRAM (seg 7)	224 KB (seg 7−B)	
		256 KB (seg 7−A)	
0x41 9998	Reserved		
0x38 0000	1536 KB Internal SRAM (seg 6)		
0x34 CCCC	Reserved		
0x30 0000	768 KB Internal SRAM (seg 5)	384 KB (seg 5−B)	
		384 KB (seg 5−A)	
0x29 9998	Reserved		
0x28 0000	256 KB Internal SRAM (seg 4)		○
0x21 9998	Reserved		
0x20 0000	256 KB Internal SRAM (seg 3)		○
0x19 9998	Reserved		
0x18 0000	256 KB Internal SRAM (seg 2)		○
0x11 9998	Reserved		
0x10 0000	256 KB Internal SRAM (seg 1)		○
0x09 9998	Reserved		
0x08 0000	256 KB Internal SRAM (seg 0)	128 KB (seg 0−B)	○
		128 KB (seg 0−A)	○
0x01 6000	Reserved		
0x00 0000	220 KB Internal SRAM (seg 9)		○

2. PM of LPDSP32 cannot access internal SRAM seg5, 6, and 7.

TERMINAL FUNCTIONS

XA: Package Code = “XA”

Table 11. TERMINAL FUNCTIONS

Terminal Name	Polarity	Direction	Function		Available(○)	
Multiplexed Function				IO POWER	XA	TBD 240pin
JTAG/SWD						
TDO	–	O	JTAG test data output	VddSD1	○	○
SDWP1	Pos	I	SD I/F Ch1 write protect		○	○
GPIO21	–	B	GPIO		○	○
EXTINT21	–	I	External Interrupt 2−bit1		○	○
TDI	–	I	JTAG test data input	VddSD1	○	○
SDCD1	Neg	I	SD I/F Ch1 detect		○	○
SWO	–	O	serial wire view data		○	○
GPIO20	–	B	GPIO		○	○
EXTINT20	–	I	External Interrupt 2−bit0		○	○
TMS	–	I	JTAG test data select	Vdd2	○	○
SDWP2	Pos	I	SD I/F Ch2 write protect		○	○
GPIO28	–	B	GPIO		○	○
EXTINT28	–	I	External Interrupt 2−bit8		○	○
TCK	Pos	I	JTAG test clock	Vdd2	○	○
SDCD2	Neg	I	SD I/F Ch2 detect		○	○
GPIO29	–	B	GPIO		○	○
EXTINT29	–	I	External Interrupt 2−bit9		○	○
SWDCLK	Pos	I	Serial wire clock	Vdd2	○	○
DMCKO0B	–	O	Digital Mic Ch0 Clock B Output		○	○
GPIO58	–	B	GPIO		○	○
EXTINT58	–	I	External Interrupt 5−bit8		○	○
SWDIO	–	B	Serial wire Data	Vdd2	○	○
DMDIN0B	–	I	Digital Mic Ch0 Data B Input		○	○
GPIO59	–	B	GPIO		○	○
EXTINT59	–	I	External Interrupt 5−bit9		○	○
Sum					6	6
RTC						
XIN32K	Pos	I	32.768KHz XTAL Input (XTRTC)	VddRTC	○	○
XOUT32K	–	O	32.768KHzXTAL Output (XTRTC)	VddRTC	○	○
VDET	Neg	I	RTC power detect Input	VddRTC	○	○
RTCINT	Neg	O	RTC Interrupt Output (Normal: Hiz, I nterrupt enabled:Low Output)	VddRTC	○	○
BACKUPB	Neg	I	RTC backup mode input Bonded with VDET internally for “XA”	VddRTC		○
KEYINT[2]	–	I	RTC KEY input can be used when KeyInt RTC mode	VddRTC		○
KEYINT[1:0]	–	I	RTC KEY input can be used when KeyInt RTC mode	VddRTC	○	○

Table 11. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function		Available(○)	
Multiplexed Function				IO POWER	XA	TBD 240pin
RTC						
RTCMODE	–	I	RTC mode input (Note 3) Set General or KeyInt RTC mode RTCMODE = “0” : KeyInt RTC mode “1” : General RTC mode Bonded to “0” internally for “XA”	VddRTC		○
VddRTC	–	P	RTC power supply	○	○	○
VssRTC	–	P	RTC ground	○	○	○
Sum					8	11
EXTERNAL INTERRUPT/GPIO						
SDRADDR12	–	O	SDRAM address	Vdd2		○
GPIO2A	–	B	GPIO			○
EXTINT2A	–	I	External Interrupt 2−bit10			○
SCL1	–	O	I2C ch1 Clock (open drain output)	Vdd2	○	○
GPIO2B	–	B	GPIO		○	○
EXTINT2B	–	I	External Interrupt 2−bit11		○	○
SDA1	–	B	I2C ch1 Data (open drain output)	Vdd2	○	○
GPIO2C	–	B	GPIO		○	○
EXTINT2C	–	I	External Interrupt 2−bit12		○	○
SDRADDR11	–	O	SDRAM address	Vdd2	○	○
DMCKO0A	–	O	Digital Mic Ch0 Clock A Output		○	○
GPIO2D	–	B	GPIO		○	○
EXTINT2D	–	I	External Interrupt 2−bit13		○	○
EXTINT2E	–	I	External Interrupt 2−bit14	Vdd2	○	○
GPIO2E	–	B	GPIO		○	○
EXTINT2F	–	I	External Interrupt 2−bit15	Vdd2	○	○
GPIO2F	–	B	GPIO * During Internal ROM boot, this terminal is used as the boot monitor signal.		○	○
Sum					5	6
SPI (SERIAL I/F CH0)						
SCK0	Neg	B	Serial I/F Ch0 Clock	Vdd2	○	○
GPIO1D	–	B	GPIO		○	○
EXTINT1D	–	I	External Interrupt 1−bit13		○	○
SDI0	–	I	Serial I/F Ch0 Data Input	Vdd2	○	○
GPIO1E	–	B	GPIO		○	○
EXTINT1E	–	I	External Interrupt 1−bit14		○	○
SDO0	–	O	Serial I/F Ch0 Data Output	Vdd2	○	○
GPIO1F	–	B	GPIO		○	○
EXTINT1F	–	I	External Interrupt 1−bit15		○	○
Sum					3	3

Table 11. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function		Available(○)	
Multiplexed Function				IO POWER	XA	TBD 240pin
S−FLASH I/F / SD I/F CH0 (Note 4)						
SFCK	Neg	O	Serial Flash I/F Clock (QSPI Clock)	Vdd2	○	○
GPIO0D	−	B	GPIO		○	○
EXTINT0D	−	I	External Interrupt 0−bit13		○	○
SDCLK0	−	O	SD I/F Ch0 Clock Output		○	○
SFDI(QIO0)	−	I(B)	Serial Flash I/F Data input (QSPI Data 0)	Vdd2	○	○
GPIO0E	−	B	GPIO		○	○
EXTINT0E	−	I	External Interrupt 0−bit14		○	○
SDAT00	−	B	SD I/F Ch0 Data0		○	○
SFDO(QIO1)	−	O(B)	Serial Flash I/F Data output (QSPI Data 1)	Vdd2	○	○
GPIO0F	−	B	GPIO		○	○
EXTINT0F	−	I	External Interrupt 0−bit15		○	○
SDAT01	−	B	SD I/F Ch0 Data1		○	○
SFWP(QIO2)	Neg	O(B)	Serial Flash I/F write protect (QSPI Data 2)	Vdd2	○	○
GPIO11	−	B	GPIO		○	○
EXTINT11	−	I	External Interrupt 1−bit1		○	○
SDAT02	−	B	SD I/F Ch0 Data2		○	○
SFHOLD(QIO3)	Neg	O(B)	Serial Flash I/F hold (QSPI Data 3)	Vdd2	○	○
GPIO12	−	B	GPIO		○	○
EXTINT12	−	I	External Interrupt 1−bit2		○	○
SDAT03	−	B	SD I/F Ch0 Data3		○	○
Sum					5	5
I2C						
SCL0	−	O	I2C ch0 Clock (open drain output)	Vdd2	○	○
GPIO07	−	B	GPIO		○	○
EXTINT07	−	I	External Interrupt 0−bit7		○	○
SDA0	−	B	I2C ch0 Data (open drain output)	Vdd2	○	○
GPIO08	−	B	GPIO		○	○
EXTINT08	−	I	External Interrupt 0−bit8		○	○
Sum					2	2

Table 11. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function		Available(○)	
Multiplexed Function				IO POWER	XA	TBD 240pin
UART						
TXD1	–	O	UART Ch1 transmit Data	Vdd2	○	○
SDAT20	–	B	SD I/F Ch2 Data 0		○	○
GPIO04	–	B	GPIO		○	○
EXTINT04	–	I	External Interrupt 0−bit4		○	○
RXD1	–	I	UART Ch1 receive Data	Vdd2	○	○
SDAT21	–	B	SD I/F Ch2 Data 1		○	○
GPIO05	–	B	GPIO		○	○
EXTINT05	–	I	External Interrupt 0−bit5		○	○
CTS1	Neg	I	UART Ch1 clear to send	Vdd2	○	○
SDAT22	–	B	SD I/F Ch2 Data 2		○	○
RXD0	–	I	UART Ch0 receive Data		○	○
GPIO56	–	B	GPIO		○	○
EXTINT56	–	I	External Interrupt 5−bit6		○	○
RTS1	Neg	O	UART Ch1 request to send	Vdd2	○	○
SDAT23	–	B	SD I/F Ch2 Data 3		○	○
TXD0	–	O	UART Ch0 transmit Data		○	○
GPIO57	–	B	GPIO		○	○
EXTINT57	–	I	External Interrupt 5−bit7		○	○
TXD2	–	O	UART Ch2 transmit Data	Vdd2	○	○
TIOCA10	–	B	MTM1 Ch0A – target signal of pulse−length−reader function – output of sentinel−inform−function – output of PWM output		○	○
GPIO0B	–	B	GPIO		○	○
EXTINT0B	–	I	External Interrupt 0−bit11		○	○
RXD2	–	I	UART Ch2 receive Data	Vdd2	○	○
TIOCA11	–	B	MTM1 Ch1A – target signal of pulse−length−reader function – output of sentinel−inform−function – output of PWM output		○	○
GPIO0C	–	B	GPIO		○	○
EXTINT0C	–	I	External Interrupt 0−bit12		○	○
			Sum		6	6
TIMER						
TIOCA00	–	B	MTM0 Ch0A – target signal of pulse−length−reader function – output of sentinel−inform−function – output of PWM output	Vdd2	○	○
SDCLK2	–	O	SD I/F Ch2 Clock Output		○	○
PHI0	–	O	System Clock Output 0		○	○
GPIO09	–	B	GPIO		○	○
EXTINT09	–	I	External Interrupt 0−bit9		○	○

Table 11. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function		Available(○)	
Multiplexed Function				IO POWER	XA	TBD 240pin
TIMER						
TIOCA01	–	B	MTM0 Ch1A – target signal of pulse–length–reader function – output of sentinel–inform–function – output of PWM output	Vdd2	○	○
SDCMD2	–	B	SD I/F Ch2 command line		○	○
PHI1	–	O	System Clock Output 1		○	○
GPIO0A	–	B	GPIO		○	○
EXTINT0A	–	I	External Interrupt 0–bit10		○	○
TIOCB00	–	B	MTM0 Ch0B – target signal of pulse–length–reader function – output of sentinel–inform–function	Vdd2	○	○
DIN1	–	I	PCM1 Data Input		○	○
DMDIN0A	–	I	Digital Mic Ch0 Data A Input		○	○
GPIO02	–	B	GPIO		○	○
EXTINT02	–	I	External Interrupt 0–bit2		○	○
TIOCB01	–	B	MTM0 Ch1B – target signal of pulse–length–reader function – output of sentinel–inform–function	Vdd2	○	○
SFQSCS	Neg	O	Serial Flash I/F QSPI chip select During Serial Flash Boot, this is used as chip select of Serial Flash		○	○
GPIO03	–	B	GPIO		○	○
EXTINT03	–	I	External Interrupt 0–bit3		○	○
SDCMD0	–	B	SD I/F Ch0 command line		○	○
TCLKA0	–	I	MTM0 external Clock A	Vdd2	○	○
BCK1	–	B	PCM1 bit Clock		○	○
GPIO00	–	B	GPIO		○	○
EXTINT00	–	I	External Interrupt 0–bit0		○	○
TCLKB0	–	I	MTM0 external Clock B	Vdd2	○	○
LRCK1	–	B	PCM1 LR Clock		○	○
GPIO01	–	B	GPIO		○	○
EXTINT01	–	I	External Interrupt 0–bit1		○	○
			Sum		6	6
PCM I/F						
MCLK0	Pos	B	PCM0 maser Clock	Vdd2	○	○
MCLK1	Pos	B	PCM1 master Clock		○	○
GPIO18	–	B	GPIO		○	○
EXTINT18	–	I	External Interrupt 1–bit8		○	○
BCK0	–	B	PCM0 bit Clock	Vdd2	○	○
DMCKO0B	–	O	Digital Mic Ch0 Clock B Output		○	○
GPIO19	–	B	GPIO		○	○
EXTINT19	–	I	External Interrupt 1–bit9		○	○

Table 11. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function		Available(○)	
Multiplexed Function				IO POWER	XA	TBD 240pin
PCM I/F						
LRCK0	–	B	PCM0 LR Clock	Vdd2	○	○
DMDIN0B	–	I	Digital Mic Ch0 Data B Input		○	○
GPIO1A	–	B	GPIO		○	○
EXTINT1A	–	I	External Interrupt 1−bit10		○	○
DIN0	–	I	PCM0 Data Input	Vdd2	○	○
DMDIN0A	–	I	Digital Mic Ch0 Data A Input		○	○
GPIO1B	–	B	GPIO		○	○
EXTINT1B	–	I	External Interrupt 1−bit11		○	○
DOUT0	–	O	PCM0 Data Output	Vdd2	○	○
DMCKO0A	–	O	Digital Mic Ch0 Clock A Output		○	○
GPIO1C	–	B	GPIO		○	○
EXTINT1C	–	I	External Interrupt 1−bit12		○	○
BCK1	–	B	PCM1 bit Clock	Vdd2	○	○
GPIO13	–	B	GPIO		○	○
EXTINT13	–	I	External Interrupt 1−bit3		○	○
LRCK1	–	B	PCM1 LR Clock	Vdd2	○	○
GPIO14	–	B	GPIO		○	○
EXTINT14	–	I	External Interrupt 1−bit4		○	○
DOUT1	–	O	PCM1 Data Output	Vdd2	○	○
GPIO15	–	B	GPIO		○	○
EXTINT15	–	I	External Interrupt 1−bit5		○	○
Sum					8	8
SD IF						
SDCLK0	–	O	SD I/F Ch0 Clock Output	Vdd2		○
SDCMD0	–	B	SD I/F Ch0 command line	Vdd2		○
SDAT0[3:0]	–	B	SD I/F Ch0 Data	Vdd2		○
SDCLK1	–	O	SD I/F Ch1 Clock Output	VddSD1	○	○
GPIO22	–	B	GPIO		○	○
EXTINT22	–	I	External Interrupt 2−bit2		○	○
SDCMD1	–	B	SD I/F Ch1 command line	VddSD1	○	○
GPIO23	–	B	GPIO		○	○
EXTINT23	–	I	External Interrupt 2−bit3		○	○
SDAT1[3:0]	–	B	SD I/F Ch1 Data	VddSD1	○	○
GPIO2[7:4]	–	B	GPIO		○	○
EXTINT2[7:4]	–	I	External Interrupt 2−bit7 to bit4		○	○
Sum					6	12
PSEUDO SRAM						
PSM_SCK	–	O	P−SRAM I/F Clock Output	Vdd2		○
PSM_CS	Neg	O	P−SRAM I/F chip select Output	Vdd2		○
PSM_SDI(DAT0)	–	I(B)	P−SRAM I/F Data input(QPI Data0)	Vdd2		○
PSM_SDO(DAT1)	–	O(B)	P−SRAM I/F Data output(QPI Data1)	Vdd2		○
PSM_DAT2	–	B	P−SRAM I/F QPI Data 2	Vdd2		○

Table 11. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available(○)	
Multiplexed Function					XA	TBD 240pin
PSEUDO SRAM						
PSM_DAT3	–	B	P−SRAM I/F QPI Data 3	Vdd2		○
Sum					0	6
SDRAM I/F						
SDRCLK	Neg	O	SDRAM Clock Output	Vdd2		○
SDRCKE	Pos	O	SDRAM Clock enable Output	Vdd2		○
SDRCS	Neg	O	SDRAM chip select Output	Vdd2		○
SDRWE	Neg	O	SDRAM write enable Output	Vdd2		○
SDRCAS	Neg	O	SDRAM CAS Output	Vdd2		○
SDRRAS	Neg	O	SDRAM RAS Output	Vdd2		○
SDRDQM[1:0]	Pos	O	SDRAM Data mask byte lane select	Vdd2		○
SDRADDR[10:0]	–	O	SDRAM address (Note 5)	Vdd2		○
SDRBA[1:0]	–	O	SDRAM bank select	Vdd2		○
SDRDATA[15:0]	–	B	SDRAM Data	Vdd2		○
Sum					0	37
EXTERNAL MEMORY I/F						
NCS0	Neg	O	chip select0	Vdd2		○
GPIO06	–	B	GPIO			○
EXTINT06	––	I	External Interrupt 0−bit6			○
NCS1	Neg	O	chip select1	Vdd2	(Note 6)	○
RXD0	–	I	UART Ch0 receive Data		○	○
GPIO10	–	B	GPIO		○	○
EXTINT10	–	I	External Interrupt 1−bit0		○	○
NRD	Neg	O	read enable	Vdd2	(Note 6)	○
GPIO17	–	B	GPIO		○	○
EXTINT17	–	I	External Interrupt 1−bit7		○	○
NWRENWRL	Neg	O	write enable, write enable low	Vdd2	(Note 6)	○
DIN0	–	I	PCM0 Data Input		○	○
GPIO30	–	B	GPIO		○	○
EXTINT30	–	I	External Interrupt 3−bit0		○	○
NHBNWRH	Neg	O	high byte select, write enable high	Vdd2	(Note 6)	○
TXD0	–	O	UART Ch0 transmit Data		○	○
DOUT0	–	O	PCM0 Data Output		○	○
GPIO31	–	B	GPIO		○	○
EXTINT31	–	I	External Interrupt 3−bit1		○	○
NLBEXA0	–	O	low byte select, address0	Vdd2	(Note 6)	○
GPIO16	–	B	GPIO		○	○
EXTINT16	–	I	External Interrupt 1−bit6		○	○
EXA[20:15]	–	O	address	Vdd2		○
GPIO4[5:0]	–	B	GPIO			○
EXTINT4[5:0]	–	I	External Interrupt 4−bit5 to bit0			○
EXA[14:9]	–	O	address	Vdd2		○
GPIO3[F:A]	–	B	GPIO			○

Table 11. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function		Available(○)	
Multiplexed Function				IO POWER	XA	TBD 240pin
EXTERNAL MEMORY I/F						
EXTINT3[F:A]	–	I	External Interrupt 3−bit15 to bit10			○
EXA[8:5]	–	O	address	Vdd2		○
GPIO3[9:6]	–	B	GPIO			○
EXTINT3[9:6]	–	I	External Interrupt 3−bit9 to bit6			○
EXA4	–	O	address	Vdd2		○
DOUT1	–	O	PCM1 Data Output			○
GPIO35	–	B	GPIO			○
EXTINT35	–	I	External Interrupt 3−bit5			○
EXA3	–	O	address	Vdd2		○
DIN1	–	I	PCM1 Data Input			○
GPIO34	–	B	GPIO			○
EXTINT34	–	I	External Interrupt 3−bit4			○
EXA[2:1]	–	O	address	Vdd2		○
GPIO3[3:2]	–	B	GPIO			○
EXTINT3[3:2]	–	I	External Interrupt 3−bit3 to bit2			○
EXD[7:0]	–	B	Data	Vdd2		○
GPIO4[D:6]	–	B	GPIO			○
EXTINT4[D:6]	–	I	External Interrupt 4−bit13 to bit6			○
EXD[15:10]	–	B	Data	Vdd2		○
GPIO5[5:0]	–	B	GPIO			○
EXTINT5[5:0]	–	I	External Interrupt 5−bit5 to bit0			○
EXD[9:8]	–	B	Data	Vdd2		○
GPIO4[F:E]	–	B	GPIO			○
EXTINT4[F:E]	–	I	External Interrupt 4−bit15 to bit14			○
Sum					5	42
XTAL, PLL						
XIN1	–	I	XTAL input (XT1)	VddXT1	○	○
XOUT1	–	O	XTAL output (XT1)	VddXT1	○	○
VddXT1	–	P	XTAL power supply (XT1)	–	○	○
VssXT1	–	P	XTAL ground (XT1)	–	○	○
XTALINFO[1: 0]	–	B	XTALINFO[1: 0] = “00” : 24MHz “01” : 12MHz “10” : 19.2MHz “11” : reserved Used for determining clock frequency setting during internal ROM boot. Bonding “00” internally for XA.	Vdd2		○
VCNT1	–	O	PLL1 VCO control	AVddPLL1		○
AVddPLL1	–	P	PLL1 analog power supply	–	○	○
AVssPLL1	–	P	PLL1 analog power ground	–	○	○
VCNT2	–	O	PLL2 VCO control	AVddPLL2		○
AVddPLL2	–	P	PLL2 analog power supply	–	○	○
AVssPLL2	–	P	PLL2 analog power ground	–	○	○

Table 11. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function		Available(○)	
Multiplexed Function				IO POWER	XA	TBD 240pin
XTAL, PLL						
Sum					8	12
USB−PHY						
USBDP	−	B	USB D+	AVddUSBPHY2	○	○
USBDM	−	B	USB D−	AVddUSBPHY2	○	○
USBEXT02	−	B	USB reference resistor	AVddUSBPHY18	○	○
USBVBUS	−	I	USB 5V VBUS detection	−	○	○
USBID	−	B	USB identifier	AVddUSBPHY18	○	○
DVddUSBPHY1	−	P	USB−PHY 1.0V digital power supply	−	○	○
AVddUSBPHY2	−	P	USB−PHY 3.3V analog power supply	−	○	○
AVddUSBPHY18	−	P	USB−PHY 1.8V analog power supply	−	○	○
AVssUSBPHY	−	P	USB−PHY ground	−	○ 2	○ 2
Sum					10	10
12 BIT ADC						
SIN[7: 3]	−	I	ADC input ch7−3	AVddADC		○
SIN[2: 0]	−	I	ADC input ch2−0	AVddADC	○	○
AVddADC	−	P	ADC analog power supply	−	○	○
AVssADC	−	P	ADC analog power ground	−	○	○
Sum					5	10
CLASS−D AMP						
LOUT	−	O	Lch Class D AMP Output	AVddDAMPL	○	○
GPLOUT	−	O	General purpose Output (GPO)		○	○
ROUT	−	O	Rch Class D AMP Output	AVddDAMPR	○	○
GPROUT	−	O	General purpose Output (GPO)		○	○
AVddDAMPL	−	P	Lch Class D AMP analog power supply	−	○	○
AVddDAMPR	−	P	Rch Class D AMP analog power supply	−	○	○
AVssDAMPL	−	P	Lch Class D AMP analog power ground	−	○	○
AVssDAMPR	−	P	Rch Class D AMP analog power ground	−	○	○
Sum					6	6
OTHER, POWER						
BMODE[1: 0]	−	B	Boot mode select	Vdd2	○	○
TEST	Pos	I	test mode Connect to ground.	VddRTC	○	○
NRES	Neg	I	SoC reset input	Vdd2	○	○
IO18V	−	I	1.8 V IO range select for I/O of Vdd2 “0” : 3.3 V IO operation “1” : 1.8 V IO operation When setting “1”, don’t supply any voltage over the 1.8 V voltage range to Vdd2.	Vdd1	○	○
Vdd1	−	P	Digital core power supply	−	○ 6	○ 7
Vdd2	−	P	Digital IO power supply	−	○ 6	○ 15

Table 11. TERMINAL FUNCTIONS (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available(○)	
Multiplexed Function					XA	TBD 240pin
OTHER, POWER						
VddSD1	–	P	Digital IO power supply(SDI/F ch1)	–	○ 1	○ 1
Vss1	–	P	Digital core power ground	–	○ 6	○ 9
Vss2	–	P	Digital IO power ground	–	○ 7	○ 15
Sum					31	52
All Sum					120	240

3. Set according to the General RTC mode or KeyInt RTC mode.
4. S−Flash I/F / SD I/F Ch0 includes SFQSCS / SDCMD0 in Timer.
5. SDRAM address bit is 13 bit including SDRADDR [12:11].
6. This function is not available.

Signals Handled by Pin Multiplex Function

The pin multiplex function can be used to assign low−speed signals to any of GPIOs. The table below shows the signal functions that can be multiplexed and the GPIOs that can be assigned.

Table 12. PIN MULTIPLEX FUNCTIONS

Number	Module name	Signal name	Function	Assigned GPIO
0	I2C0	SCL0	I2C ch0 Clock	GPIO00 to 0F GPIO10 to 1F GPIO20 to 2F GPIO30 to 3F GPIO40 to 4F GPIO50 to 59
1		SDA0	I2C ch0 Data	
2	I2C1	SCL1	I2C ch1 Clock	
3		SDA1	I2C ch1 Data	
4	SPI0	SCK0	Serial I/F Ch0 Clock	
5		SDI0	Serial I/F Ch0 Data Input	
6		SDO0	Serial I/F Ch0 Data Output	
7	SPI1	SCK1	Serial I/F Ch1 Clock	
8		SDI1	Serial I/F Ch1 Data Input	
9		SDO1	Serial I/F Ch1 Data Output	
10	MTM0	TCLKA0	MTM0 external Clock A	
11		TCLKB0	MTM0 external Clock B	
12		TIOCA00	MTM0 Ch0A	
13		TIOCA01	MTM0 Ch1A	
14		TIOCB00	MTM0 Ch0B	
15		TIOCB01	MTM0 Ch1B	
16	MTM1	TCLKA1	MTM1 external Clock A	
17		TCLKB1	MTM1 external Clock B	
18		TIOCA10	MTM1 Ch0A	
19		TIOCA11	MTM1 Ch1A	
20		TIOCB10	MTM1 Ch0B	
21		TIOCB11	MTM1 Ch1B	
22	UART0	RXD0	UART Ch0 receive Data	
23		TXD0	UART Ch0 transmit Data	
24	UART1	RXD1	UART Ch1 receive Data	
25		TXD1	UART Ch1 transmit Data	
26		CTS1	UART Ch1 clear to send	
27		RTS1	UART Ch1 request to send	
28	UART2	RXD2	UART Ch2 receive Data	
29		TXD2	UART Ch2 transmit Data	
30		CTS2	UART Ch2 clear to send	
31		RTS2	UART Ch2 request to send	
32	DMIC0	DMCKO0	Digital Mic Ch0 Clock Output	
33		DMDIN0	Digital Mic Ch0 Data Input	
34	DMIC1	DMCKO1	Digital Mic Ch1 Clock Output	
35		DMDIN1	Digital Mic Ch1 Data Input	
36	OSC	WICPOWERDOWN	Power control for WIC Sleep	
37	Reserved	Reserved	Reserved	

Boot Mode

The available boot modes are determined by the values on the BMODE[1:0] terminal.

Table 13. BOOT MODE

IPL mode	BMODE1	BMODE0	Explanation
Physical Boot USB	PD 470 kΩ	PD 470 kΩ	Internal ROM boot (EMMC Physical Boot with USB download) (SD card I/F Ch0 + USB Device + EXTINT2F)
			IPL2 is transferred to boot partition1 area of eMMC via USB from PC. Using Boot operation mode of eMMC, IPL2(program) is copied to internal SRAM from boot partition1 area of eMMC connected to SDCH0 and is executed. XT1 must be connected in this mode to boot the ROM. The connection of XTRTC is arbitrary.
Physical Boot SD	PD 470 kΩ	PU 470 kΩ	Internal ROM boot (EMMC Physical Boot with SD Ch1 download) (SD card I/F Ch0 + SD card I/F Ch1 + EXTINT2F)
			IPL2 is transferred to boot partition1 area of eMMC from SDCH1. Using Boot operation mode of eMMC, IPL2(program) is copied to internal SRAM from boot partition1 area of eMMC connected to SDCH0 and is executed. Either XT1 or XTRTC is required to boot the ROM.
User Area Boot USB	PD 1 kΩ	PU or PD 470 kΩ	Internal ROM boot (User Area Boot with USB download) (SD card I/F Ch0 + USB Device + EXTINT2F)
			IPL2 is transferred to user area of eMMC via USB from PC. IPL2(program) is copied to internal SRAM from user area of eMMC connected to SDCH0 and is executed. XT1 must be connected in this mode to boot the ROM. The connection of XTRTC is arbitrary.
User Area Boot SD	PU 470 kΩ	PD 1 kΩ	Internal ROM boot (User Area Boot with SD Ch1 download) (SD card I/F Ch0 + SD card I/F Ch1 + EXTINT2F)
			IPL2 is transferred to user area of eMMC from SDCH1. IPL2(program) is copied to internal SRAM from user area of eMMC connected to SDCH0 and is executed. Either XT1 or XTRTC is required to boot the ROM.
SPI Boot USB	PU 470 kΩ	PU 470 kΩ	Internal ROM boot (External Serial Flash SPI Boot with USB download) (S−FLASH I/F + USB Device + EXTINT2F)
			IPL2 is transferred to user area of S−FLASH via USB from PC. IPL2(program) is copied to internal SRAM from user area of S−FLASH and is executed. XT1 must be connected in this mode to boot the ROM. The connection of XTRTC is arbitrary.
SPI Boot SD	PD 470 kΩ	PU 1 kΩ	Internal ROM boot (External Serial Flash SPI Boot with SD Ch1 download) (S−FLASH I/F + SDcard I/F Ch1 + EXTINT2F)
			IPL2 is transferred to user area of S−FLASH from SDCH1. IPL2(program) is copied to internal SRAM from user area of S−FLASH and is executed. Either XT1 or XTRTC is required to boot the ROM.
QSPI Boot USB	PU 1 kΩ	PU 470 kΩ	Internal ROM boot (External Serial Flash QSPI Boot with USB download) (S−Flash I/F(QSPI) + USB Device + EXTINT2F)
			The IPL supports the direct write of the program using the DD command from USB. In this mode, the CPU fetches Serial Flash connected to S/Flash IF directly. XT1 must be connected in this mode to boot the ROM. The connection of XTRTC is arbitrary.

Table 13. BOOT MODE (continued)

IPL mode	BMODE1	BMODE0	Explanation
QSPI Boot SD	PU 1 kΩ	PD 470 kΩ	Internal ROM boot (External Serial Flash QSPI Boot with SD Ch1 download) (S−Flash I/F(QSPI) + SD card I/F Ch1 + EXTINT2F)
			IPL2 is transferred to S−FLASH from SDCH1. In this mode, the CPU fetches from Serial Flash connected to S/Flash IF directly. Either XT1 or XTRTC is required to boot the ROM.
User Area Delete	PD 1 kΩ	PU 1 kΩ	Internal ROM boot (User Area IPL2 deletion) (SD card I/F Ch0 + EXTINT2F)
			It comes to be able to write IPL2 again at User Area Boot. Either XT1 or XTRTC is necessary to boot the ROM.
Partition Delete	PD 470 kΩ	PD 1 kΩ	Internal ROM boot (Partition Area IPL2 deletion) (SD card I/F Ch0 + EXTINT2F)
			It comes to be able to write IPL2 again at eMMC Physical Boot. Either XT1 or XTRTC is necessary to boot the ROM.
SPI All Erase	PU 470 kΩ	PU 1 kΩ	Internal ROM boot (All external Serial Flash SPI area deletion) (S−Flash I/F, + EXTINT2F)
			All of Serial Flash is deleted. Please select it when you use Serial Flash with SPI. Either XT1 or XTRTC is required to boot the ROM.
SDCH0 All Erase	PD 1 kΩ	PD 1 kΩ	Internal ROM boot (All area deletion) (SD card I/F Ch0 + EXTINT2F)
			All of eMMC is deleted. The partition area is also erased, which takes time. When eMMC corresponds to Trim, Trim is done. Either XT1 or XTRTC is required to boot the ROM.
QSPI All Erase	PU 1 kΩ	PD 1 kΩ	Internal ROM boot (All external Serial Flash QSPI area deletion) (S−Flash I/F(QSPI) + EXTINT2F)
			All of Serial Flash is deleted. Please use it when you use Serial Flash in the fetch mode of QSPI. Either XT1 or XTRTC is required to boot the ROM.
External ROM Boot	PU 470 kΩ	PD 470 kΩ	External memory boot (External−0)
			In this mode, the CPU fetches external memory connected by the external memory controller of External0 directly. Either XT1 or XTRTC is required to boot the ROM.
Hi−z	PU 1 kΩ	PU 1 kΩ	External memory I/F terminal are Hiz EXA[20:1], EXD[15:0], NCS[1:0], NRD, NWRENWRL, NHBNWRH, NLBEXA0 SD card I/F Ch0 terminal are Hiz SDCLK0, SDCMD0, SDAT0[3:0] S−Flash(QSPI) terminal are Hiz SFQSCS, SFCK, SFDI(QIO0), SFDO(QIO1), SFWP(QIO2), SFHOLD(QIO3) Either XT1 or XTRTC is required to boot the ROM.

Boot Port

The ports used while booting are described below.

- There is no dedicated SDCH0 pin in the WLP package. Therefore, when booting from eMMC, the terminals SFCK, SFQSCS, SFDO, SFDI, SFWP, and SFHOLD must be switched to SDCLK0, SDCMD0, SDAT00, SDAT01, SDAT02, and SDAT03. The target is Physical Boot USB · Physical Boot SD · User Area Boot USB · User Area Boot SD · User Area Delete, Partition Delete, SDCH 0 All Erase
- SD Card SDCH1 uses only CMD, DATA, and CLK. The terminals CD and WP are not used. These three terminals are controlled only when writing IPL2 from SDCH1
- SPI Boot / SPI All Erase uses only SFCK, SFDO, SFDI and SFQSCS switched from TIOCB01. SFHOLD and SFWP (The function is different according to the device) are not used
- QSPI Boot / QSPI All Erase uses SFCK, SFDO, SFDI, SFHOLD, SFWP and SFQSCS switched from TIOCB01
- External ROM boot uses NCS0 and other terminals required by the external memory controller

Table 14. GPIOs USED DURING IPL

IPL mode	Package	
	XA	TBD(240pin)
Physical Boot USB	P2F(error notification) P0D(SDCLK0), P0E(SDAT00), P0F(SDAT01), P11(SDAT02), P12(SDAT03), P03(SCMD0)	P2F(error notification)
Physical Boot SD	P2F(error notification), P22(SDCLK1), P23(SDCMD1), P24(SDDATA10), P25(SDDATA11), P26(SDDATA12), P27(SDDATA13), P0D(SDCLK0), P0E(SDAT00), P0F(SDAT01), P11(SDAT02), P12(SDAT03) P03(SCMD0)	P2F(error notification), P22(SDCLK1), P23(SDCMD1), P24(SDDATA10), P25(SDDATA11), P26(SDDATA12), P27(SDDATA13)
User Area Boot USB	P2F(error notification), P0D(SDCLK0), P0E(SDAT00), P0F(SDAT01), P11(SDAT02), P12(SDAT03), P03(SCMD0)	P2F(error notification)
User Area Boot SD	P2F(error notification) P0D(SDCLK0), P0E(SDAT00), P0F(SDAT01), P11(SDAT02), P12(SDAT03), P03(SCMD0), P22(SDCLK1), P23(SDCMD1), P24(SDDATA10), P25(SDDATA11), P26(SDDATA12), P27(SDDATA13)	P2F(error notification), P22(SDCLK1), P23(SDCMD1), P24(SDDATA10), P25(SDDATA11), P26(SDDATA12), P27(SDDATA13)
SPI Boot USB	P2F(error notification) P0D(SFCK), P03(SFQSCS), P0F(SFDO), P0E(SFDI)	P2F(error notification), P0D(SFCK), P03(SFQSCS), P0F(SFDO), P0E(SFDI)
SPI Boot SD	P2F(error notification), P0D(SFCK), P03(SFQSCS) P0F(SFDO), P0E(SFDI), P22(SDCLK1), P23(SDCMD1), P24(SDDATA10), P25(SDDATA11), P26(SDDATA12), P27(SDDATA13)	P2F(error notification), P0D(SFCK), P03(SFQSCS) P0F(SFDO), P0E(SFDI), P22(SDCLK1), P23(SDCMD1), P24(SDDATA10), P25(SDDATA11), P26(SDDATA12), P27(SDDATA13)
QSPI Boot USB	P2F(error notification), P0D(SFCK), P03(SFQSCS), P0F(SFDO), P0E(SFDI), P11(SFWP), P12(SFHOLD)	P2F(error notification), P0D(SFCK), P03(SFQSCS), P0F(SFDO), P0E(SFDI), P11(SFWP), P12(SFHOLD)
QSPI Boot SD	P2F(error notification) P0D(SFCK), P03(SFQSCS), P0F(SFDO), P0E(SFDI), P011(SFWP), P12(SFHOLD), P22(SDCLK1), P23(SDCMD1), P24(SDDATA10), P25(SDDATA11), P26(SDDATA12), P27(SDDATA13)	P2F(error notification) P0D(SFCK), P03(SFQSCS), P0F(SFDO), P0E(SFDI), P011(SFWP), P12(SFHOLD), P22(SDCLK1), P23(SDCMD1), P24(SDDATA10), P25(SDDATA11), P26(SDDATA12), P27(SDDATA13)
UserArea Delete	P2F(error notification), P0D(SDCLK0), P0E(SDAT00), P0F(SDAT01), P11(SDAT02), P12(SDAT03), P03(SCMD0)	P2F(error notification)
Partition Delete	P2F(error notification), P0D(SDCLK0), P0E(SDAT00), P0F(SDAT01), P11(SDAT02), P12(SDAT03), P03(SCMD0)	P2F(error notification)

Table 14. GPIOs USED DURING IPL (continued)

IPL mode	Package	
	XA	TBD(240pin)
SPI Erase	P2F(error notification), P0D(SFCK), P03(SFQSCS), P0F(SPIOUT), P0E(SFDI)	P2F(error notification), P0D(SFCK), P03(SFQSCS), P0F(SPIOUT), P0E(SFDI)
SDCH0 All Erase	P2F(error notification), P0D(SDCLK0), P0E(SDAT00), P0F(SDAT01), P11(SDAT02), P12(SDAT03), P03(SCMD0)	P2F(error notification)
QSPI All Erase	P2F(error notification), P0D(SFCK), P03(SFQSCS), P0F(SFDO), P0E(SFDI), P11(SFWP), P12(SFHOLD)	P2F(error notification), P0D(SFCK), P03(SFQSCS), P0F(SFDO), P0E(SFDI), P11(SFWP), P12(SFHOLD)
External ROM Boot	N/A	P06(NCS0), P17(NRD), P30(NWRENWRL) P31(NHBNWRH), P16(NLBEXA0), P32(EXA01), P33(EXA02), P34(EXA03), P35(EXA06), P36(EXA05), P37(EXA06), P38(EXA07), P39(EXA08), P3A(EXA09), P3B(EXA10), P3C(EXA11), P3D(EXA12), P3E(EXA13), P3F(EXA14), P40(EXA15), P41(EXA16), P42(EXA17), P43(EXA18), P44(EXA19), P45(EXA20), P46(EXD00), P47(EXD01), P48(EXD02), P49(EXD03), P4A(EXD04), P4B(EXD05), P4C(EXD06), P4D(EXD07), P4E(EXD08), P4F(EXD09), P50(EXD10), P51(EXD11), P52(EXD12), P53(EXD13), P54(EXD14), P55(EXD15)
HI−z		SDCLK0 is set to the Hi−z input.

7. In this table, “Pxx” means “GPIOxx”. For example “P2F” means “GPIO2F”.

SDIF PullUp

If using the SDIF port during boot mode, internal PullUp resistors are used (SDCMD0, SDAT0[3:0] / SDCMD1, SDAT1[3:0]). Therefore, external PullUp resistors are not required on the board.

SFQSCS PullUp

If using SFQSCS during boot mode, the initial condition for terminal P03 relative to SFQSCS us Pull−Up. After terminal P03 is switched to SFQSCS, the Pull−Up is released.

GPIO2F

During boot mode, GPIO2F provides notification of the beginning of USB connection, notification of the termination of USB connection, as well as error notification with High/Low of the terminal.

When errors occur during boot sequences, for example writing of IPL2, GPIO2F reports the sort of error. Moreover, GPIO2F can indicate the status of USB connection and the completion of USB file transfer. Additionally, Delete Mode, completion of Erase, and status of Erase can also be reported through a sequence of Low/High.

For more detail about the behavior of this port used during boot, refer to the “IPL detail” chapter in the ”LC823455 Sample Software Reference”.

PIN ASSIGNMENT

Table 15. PIN ASSIGNMENT

I/O	
I	Input
O	Output
B	Bidirectional
P	Power
G	Ground

Table 16.

TBD 240pin		WLP120		PIN NAME	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No	Ball								
1		–	–	Vdd2	P						
2		–	–	Vss2	G						
3		–	–	EXD0/ GPIO46/ EXTINT46	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
4		–	–	EXA1/ GPIO32/ EXTINT32	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
5		–	–	EXA11/ GPIO3C/ EXTINT3C	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
6		–	–	EXA12/ GPIO3D/ EXTINT3D	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
7		–	–	EXA13/ GPIO3E/ EXTINT3E	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
8		–	–	EXA14/ GPIO3F/ EXTINT3F	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
9		1	L10	Vdd1	P						
10		2	H8	NRD/ GPIO17/ EXTINT17	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
11		3	K9	SWDIO/ DMDIN0B/ GPIO59/ EXTINT59	B/ I/ B/ I	Schmitt	3−State	2 mA	PU	Vdd2	3ISU/3T2
12		4	G7	NLBEXA0/ GPIO16/ EXTINT16	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
13		–	–	EXD2/ GPIO48/ EXTINT48	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
14		–	–	EXA2/ GPIO33/ EXTINT33	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
15		5	L9	Vss2	G						
16		–	–	EXA6/ GPIO37/ EXTINT37	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
17		–	–	EXA7/ GPIO38/ EXTINT38	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
18		–	–	SDRADDR12/ GPIO2A/ EXTINT2A	O/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
19		6	J8	TDI/ SDCD1/ SWO/ GPIO20/ EXTINT20	I/ I/ O/ B/ I	Schmitt	3−State	2 mA	PU/PD	VddSD1	3ISUD/3T2

Table 16. (continued)

TBD 240pin		WLP120		PIN NAME	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No	Ball								
20		7	K8	TDO/ SDWP1/ GPIO21/ EXTINT21	O/ I/ B/ I	Schmitt	3−State	2 mA	PU/PD	VddSD1	3ISUD/3T2
21		8	L8	VddSD1	P						
22		9	H7	SDCMD1/ GPIO23/ EXTINT23	B/ B/ I	CMOS	3−State	2/4/8/10 mA	PU/PD	VddSD1	3ICUD/3T2 (4)(8)(10)
23		10	J7	SDAT10/ GPIO24/ EXTINT24	B/ B/ I	CMOS	3−State	2/4/8/10mA	PU/PD	VddSD1	3ICUD/3T2 (4)(8)(10)
24		11	K7	SDAT11/ GPIO25/ EXTINT25	B/ B/ I	CMOS	3−State	2/4/8/10mA	PU/PD	VddSD1	3ICUD/3T2 (4)(8)(10)
25		12	L7	Vss2	G						
26		13	F5	SDAT12/ GPIO26/ EXTINT26	B/ B/ I	CMOS	3−State	2/4/8/10mA	PU/PD	VddSD1	3ICUD/3T2 (4)(8)(10)
27		14	G6	SDAT13/ GPIO27/ EXTINT27	B/ B/ I	CMOS	3−State	2/4/8/10mA	PU/PD	VddSD1	3ICUD/3T2 (4)(8)(10)
28		15	H6	SDCLK1/ GPIO22/ EXTINT22	O/ B/ I	CMOS	3−State	2/4/8/10mA	PU/PD	VddSD1	3ICUD/3T2 (4)(8)(10)
29		16	L6	Vss1	G						
30		−	−	RTCMODE	I	CMOS	−	−	−	VddRTC	1IC
31		17	K6	VddRTC	P						
32		18	J5	XIN32K	I	X	−	−	−	VddRTC	X
33		19	K5	VssRTC	G						
34		20	L5	XOUT32K	O	−	X	−	−	VddRTC	X
35		−	−	Keyint2	I	CMOS	−	−	PD	VddRTC	1ICD
36		−	−	BACKUPB	I	CMOS	−	−	−	VddRTC	1IC
37		21	J6	VDET	I	CMOS	−	−	−	VddRTC	1IC
38		22	H5	RTCINT (Note 8)	O	−	OD	0.3 mA−OD	−	VddRTC	OD3
39		23	G5	Keyint0	I	CMOS	−	−	PD	VddRTC	1ICD
40		24	H4	TEST	I	CMOS	−	−	−	VddRTC	1IC
41		25	L4	Keyint1	I	CMOS	−	−	PD	VddRTC	1ICD
42		26	K4	AVddPLL1	P						
43		−	−	VCNT1	O	−	1A	−	−	AVddPLL1	1A
44		27	J4	AVssPLL1	G						
45		28	K3	AVddPLL2	P						
46		−	−	VCNT2	O	−	1A	−	−	AVddPLL2	1A
47		29	L3	AVssPLL2	G						
48		−	−	Vss1	G						
49		−	−	Vdd2	P						
50		−	−	Vss2	G						
51		−	−	EXD4/ GPIO4A/ EXTINT4A	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
52		−	−	EXD5/ GPIO4B/ EXTINT4B	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
53		30	L2	Vdd1	P						
54		−	−	EXD6/ GPIO4C/ EXTINT4C	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)

Table 16. (continued)

TBD 240pin		WLP120		PIN NAME	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No	Ball								
55		–	–	EXA19/ GPIO44/ EXTINT44	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
56		–	–	EXA20/ GPIO45/ EXTINT45	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
57		–	–	EXD7/ GPIO4D/ EXTINT4D	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
58		–	–	EXD8/ GPIO4E/ EXTINT4E	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
59		31	L1	Vss1	G						
60		–	–	EXD11/ GPIO51/ EXTINT51	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
61		–	–	EXD12/ GPIO52/ EXTINT52	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
62		–	–	EXD13/ GPIO53/ EXTINT53	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
63		–	–	EXD14/ GPIO54/ EXTINT54	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
64		–	–	Vss2	G						
65		32	K2	DOUT1/ GPIO15/ EXTINT15	O/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
66		–	–	EXD9/ GPIO4F/ EXTINT4F	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
67		–	–	EXD10/ GPIO50/ EXTINT50	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
68		33	K1	Vdd2	P						
69		–	–	EXD15/ GPIO55/ EXTINT55	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
70		34	J3	BCK1/ GPIO13/ EXTINT13	B/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
71		35	G4	MCLK0/ MCLK1/ GPIO18/ EXTINT18	B/ B/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
72		36	J2	LRCK1/ GPIO14/ EXTINT14	B/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
73		37	J1	Vss2	G						
74		–	–	Vdd2	P						
75		38	H3	BCK0/ DMCKO0B/ GPIO19/ EXTINT19	B/ O/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
76		39	G3	LRCK0/ DMDIN0B/ GPIO1A/ EXTINT1A	B/ I/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
77		40	H2	DIN0/ DMDIN0A/ GPIO1B/ EXTINT1B	I/ I/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
78		–	–	Vss2	G						
79		–	–	XTALINFO1	B	Schmitt	3−State	2/4/8 mA	PU	Vdd2	3ISU/3T2 (4)(8)
80		–	–	Vdd2	P						

Table 16. (continued)

TBD 240pin		WLP120		PIN NAME	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No	Ball								
81		41	H1	DOUT0/ DMCKO0A GPIO1C/ EXTINT1C	O/ O/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
82		42	F4	BMODE0	B	Schmitt	3−State	2 mA	PU/PD	Vdd2	3ISUD/3T2
83		43	F3	BMODE1	B	Schmitt	3−State	2 mA	PU/PD	Vdd2	3ISUD/3T2
84		−	−	SDRADDR1	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
85		−	−	EXA4/ DOUT1/ GPIO35/ EXTINT35	O/ O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
86		−	−	SDRADDR0	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
87		44	G1	NRES	I	Schmitt	−	−	−	Vdd2	3IS
88		45	G2	AVssDAMPR	G						
89		46	F1	ROUT/ GPROUT	O/ O	−	1A	−	−	AVddDAMPR	1A
90		47	F2	AVddDAMPR	P						
91		48	E2	AVddDAMPL	P						
92		49	E1	LOUT/ GPLOUT	O/ O	−	1A	−	−	AVddDAMPL	1A
93		50	D2	AVssDAMPL	G						
94		51	D1	Vss1	G						
95		−	−	SDRADDR2	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
96		−	−	SDRADDR3	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
97		52	E3	SCL1/ GPIO2B/ EXTINT2B	O/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
98		53	E4	SDA1/ GPIO2C/ EXTINT2C	B/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
99		54	D3	SDRADDR11/ DMCKO0A/ GPIO2D/ EXTINT2D	O/ O/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
100		−	−	SDRDATA0	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
101		55	C1	Vdd1	P						
102		−	−	SDRDATA1	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
103		56	C2	TCLKA0/ BCK1/ GPIO00/ EXTINT00	I/ B/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
104		57	D4	TCLKB0/ LRCK1/ GPIO01/ EXTINT01	I/ B/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
105		58	C3	NHBNWRH/ TXD0/ DOUT0/ GPIO31/ EXTINT31	O/ O/ O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
106		−	−	Vdd2	P						
107		59	B1	Vss2	G						
108		−	−	PSM_DAT2	B	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
109		−	−	PSM_SDO (DAT1)	O(B)	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
110		−	−	PSM_DAT3	B	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)

Table 16. (continued)

TBD 240pin		WLP120		PIN NAME	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No	Ball								
111		–	–	SDRADDR4	O	–	3−State	2/4/8 mA	–	Vdd2	3T2(4)(8)
112		–	–	SDRDATA4	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
113		–	–	SDRDATA14	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
114		60	A1	Vdd2	P						
115		–	–	Vdd2	P						
116		–	–	SDRDATA2	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
117		–	–	SDRDATA3	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
118		–	–	SDRDATA15	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
119		–	–	PSM_SDI (DAT0)	I(B)	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
120		–	–	PSM_CS	O	CMOS	3−State	2/4/8/10mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
121		–	–	PSM_SCK	O	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
122		–	–	SDRADDR7	O	–	3−State	2/4/8 mA	–	Vdd2	3T2(4)(8)
123		–	–	SDRDATA5	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
124		–	–	SDRDATA13	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
125		61	A2	Vss2	G						
126		62	B2	EXTINT2E/GPIO 2E	I/B	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
127		63	B3	NCS1/ RXD0/ GPIO10/ EXTINT10	O/ I/ B/ I	Schmitt	3−State	2/4/8 mA	PU	Vdd2	3ISU/3T2 (4)(8)
128		–	–	SDRDATA12	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
129		–	–	SDRDATA6	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
130		–	–	SDRDATA7	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
131		64	A3	Vss1	G						
132		–	–	SDRDATA8	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
133		65	C4	EXTINT2F/ GPIO2F	I/ B	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
134		66	B4	TCK/ SDCD2/ GPIO29/ EXTINT29	I/ I/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
135		–	–	SDRDATA9	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
136		67	A4	Vdd2	P						
137		–	–	SDRDATA11	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
138		–	–	SDRDATA10	B	CMOS	3−State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)

Table 16. (continued)

TBD 240pin		WLP120		PIN NAME	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No	Ball								
139		68	D5	TIOCA01/ SDCMD2/ PHI1/ GPIO0A/ EXTINT0A	B/ B/ O/ B/ I	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
140		69	C5	TXD1/ SDAT20/ GPIO04/ EXTINT04	O/ B/ B/ I	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
141		70	B5	RXD1/ SDAT21/ GPIO05/ EXTINT05	I/ B/ B/ I	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
142		−	−	Vss2	G						
143		71	A5	Vdd1	P						
144		72	E5	CTS1/ SDAT22/ RXD0/ GPIO56/ EXTINT56	I/ B/ I/ B/ I	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
145		73	C6	RTS1/ SDAT23/ TXD0/ GPIO57/ EXTINT57	O/ B/ O/ B/ I	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
146		74	B6	TIOCA00/ SDCLK2/ PHI0/ GPIO09/ EXTINT09	B/ O/ O/ B/ I	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
147		−	−	SDRADDR5	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
148		−	−	SDRADDR6	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
149		−	−	SDRADDR9	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
150		75	A6	Vdd2	P						
151		76	D6	TMS/ SDWP2/ GPIO28/ EXTINT28	I/ I/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
152		77	E6	TXD2/ TIOCA10/ GPIO0B/ EXTINT0B	O/ B/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
153		78	D7	RXD2/ TIOCA11/ GPIO0C/ EXTINT0C	I/ B/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
154		−	−	SDRBA1	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
155		−	−	SDRBA0	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
156		79	A7	Vss2	G						
157		−	−	SDRADDR10	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
158		80	B7	SFCK/ GPIO0D/ EXTINT0D/ SDCLK0	O/ B/ I/ O	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
159		81	C7	TIOCB01/ SFQSCS/ GPIO03/ EXTINT03/ SDCMD0	B/ O/ B/ I/ B	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
160		82	E7	SFDO(QIO1)/ GPIO0F/ EXTINT0F/ SDAT01	O(B)/ B/ I/ B	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
161		−	−	SDRRAS	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
162		83	A8	Vdd2	P						

Table 16. (continued)

TBD 240pin		WLP120		PIN NAME	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No	Ball								
163		84	B8	SFDI(QIO0)/ GPIO0E/ EXTINT0E/ SDAT00	I(B)/ B/ I/ B	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
164		85	C8	SFWP(QIO2)/ GPIO11/ EXTINT11/ SDAT02	O(B)/ B/ I/ B	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
165		86	D8	SFHOLD(QIO3)/ GPIO12/ EXTINT12/ SDAT03	O(B)/ B/ I/ B	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
166		87	A9	Vss1	G						
167		−	−	SDRWE	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
168		−	−	SDRCKE	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
169		88	B9	TIOCB00/ DIN1/ DMDIN0A/ GPIO02/ EXTINT02	B/ I/ I/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
170		−	−	SDRCLK	O	−	3−State	2/4/8/10 mA	−	Vdd2	3T2(4)(8)(10)
171		−	−	SDRCS	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
172		89	A10	IO18V	I	1A	−	−	−	Vdd1	1A
173		−	−	Vss1	G						
174		−	−	SDAT02	B	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
175		−	−	SDAT03	B	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
176		−	−	SDAT01	B	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
177		−	−	Vdd2	P						
178		−	−	Vss2	G						
179		90	A11	Vdd1	P						
180		−	−	SDRDQM1	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
181		−	−	SDAT00	B	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
182		−	−	SDCLK0	O	−	3−State	2/4/8/10 mA	−	Vdd2	3T2(4)(8)(10)
183		−	−	SDCMD0	B	CMOS	3−State	2/4/8/10 mA	PU/PD	Vdd2	3ICUD/3T2 (4)(8)(10)
184		−	−	SDRADDR8	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
185		−	−	SDRCAS	O	−	3−State	2/4/8 mA	−	Vdd2	3T2(4)(8)
186		−	−	Vdd2	P						
187		−	−	Vss2	G						
188		91	B11	SIN0	I	3A	−	−	−	AvddADC	3A
189		92	B10	SIN1	I	3A	−	−	−	AvddADC	3A
190		93	C9	SIN2	I	3A	−	−	−	AvddADC	3A
191		94	C11	AVddADC	P						
192		−	−	SIN3	I	3A	−	−	−	AvddADC	3A
193		−	−	SIN4	I	3A	−	−	−	AvddADC	3A
194		−	−	SIN5	I	3A	−	−	−	AvddADC	3A
195		−	−	SIN6	I	3A	−	−	−	AvddADC	3A
196		−	−	SIN7	I	3A	−	−	−	AvddADC	3A
197		95	C10	AVssADC	G						
198		96	E8	AVssUSBPHY	G						

Table 16. (continued)

TBD 240pin		WLP120		PIN NAME	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No	Ball								
199		97	D11	USBEXT02	B	3A	3A	–	–	AVddUSBPHY18	3A
200		98	D9	AVddUSBPHY2	P						
201		99	D10	USBDM	B	3A	3A	–	–	AVddUSBPHY2	3A
202		100	E9	AVssUSBPHY	G						
203		101	E10	USBDP	B	3A	3A	–	–	AVddUSBPHY2	3A
204		102	F8	DVddUSBPHY1	P						
205		103	F9	USBVBUS	I		–	–	–		
206		104	F10	AVddUSBPHY18	P						
207		105	F11	USBID	B	3A	3A	–	–	AVddUSBPHY18	3A
208		106	G8	VddXT1	P						
209		107	G9	XIN1	I	X	–	–	–	VddXT1	X
210		108	G10	VssXT1	G						
211		109	G11	XOUT1	O	–	X	–	–	VddXT1	X
212		–	–	Vss1	G						
213		–	–	Vdd1	P						
214		–	–	Vdd2	P						
215		–	–	XTALINFO0	B	Schmitt	3−State	2/4/8 mA	PU	Vdd2	3ISU/3T2 (4)(8)
216		–	–	Vss2	G						
217		110	F7	SDO0/ GPIO1F/ EXTINT1F	O/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
218		111	F6	SCK0/ GPIO1D/ EXTINT1D	B/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
219		–	–	SDRDQM0	O	–	3−State	2/4/8 mA	–	Vdd2	3T2(4)(8)
220		–	–	EXA15/ GPIO40/ EXTINT40	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
221		112	H11	Vdd1	P						
222		–	–	EXA10/ GPIO3B/ EXTINT3B	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
223		–	–	EXA3/ DIN1/ GPIO34/ EXTINT34	O/ I/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
224		–	–	EXA17/ GPIO42/ EXTINT42	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
225		–	–	EXD3/ GPIO49/ EXTINT49	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
226		–	–	EXA16/ GPIO41/ EXTINT41	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
227		–	–	EXA18/ GPIO43/ EXTINT43	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
228		113	J11	Vss2	G						
229		114	H10	SCL0/ GPIO07/ EXTINT07	O/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
230		115	J10	SDI0/ GPIO1E/ EXTINT1E	I/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
231		116	H9	SDA0/ GPIO08/ EXTINT08	B/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)

Table 16. (continued)

TBD 240pin		WLP120		PIN NAME	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No	Ball								
232		–	–	EXA9/ GPIO3A/ EXTINT3A	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
233		–	–	NCS0/ GPIO06/ EXTINT06	O/ B/ I	Schmitt	3−State	2/4/8 mA	PU	Vdd2	3ISU/3T2 (4)(8)
234		117	K11	Vdd2	P						
235		–	–	EXD1/ GPIO47/ EXTINT47	B/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
236		–	–	EXA5/ GPIO36/ EXTINT36	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
237		–	–	EXA8/ GPIO39/ EXTINT39	O/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
238		118	J9	NWRENWRL/ DIN0/ GPIO30/ EXTINT30	O/ I/ B/ I	Schmitt	3−State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
239		119	K10	SWDCLK/ DMCKO0B GPIO58/ EXTINT58	I/ O/ B/ I	Schmitt	3−State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)
240		120	L11	Vss1	G						

8. RTCINT (open drain Output) 3.6 V tolerant.

INPUT/OUTPUT CIRCUIT

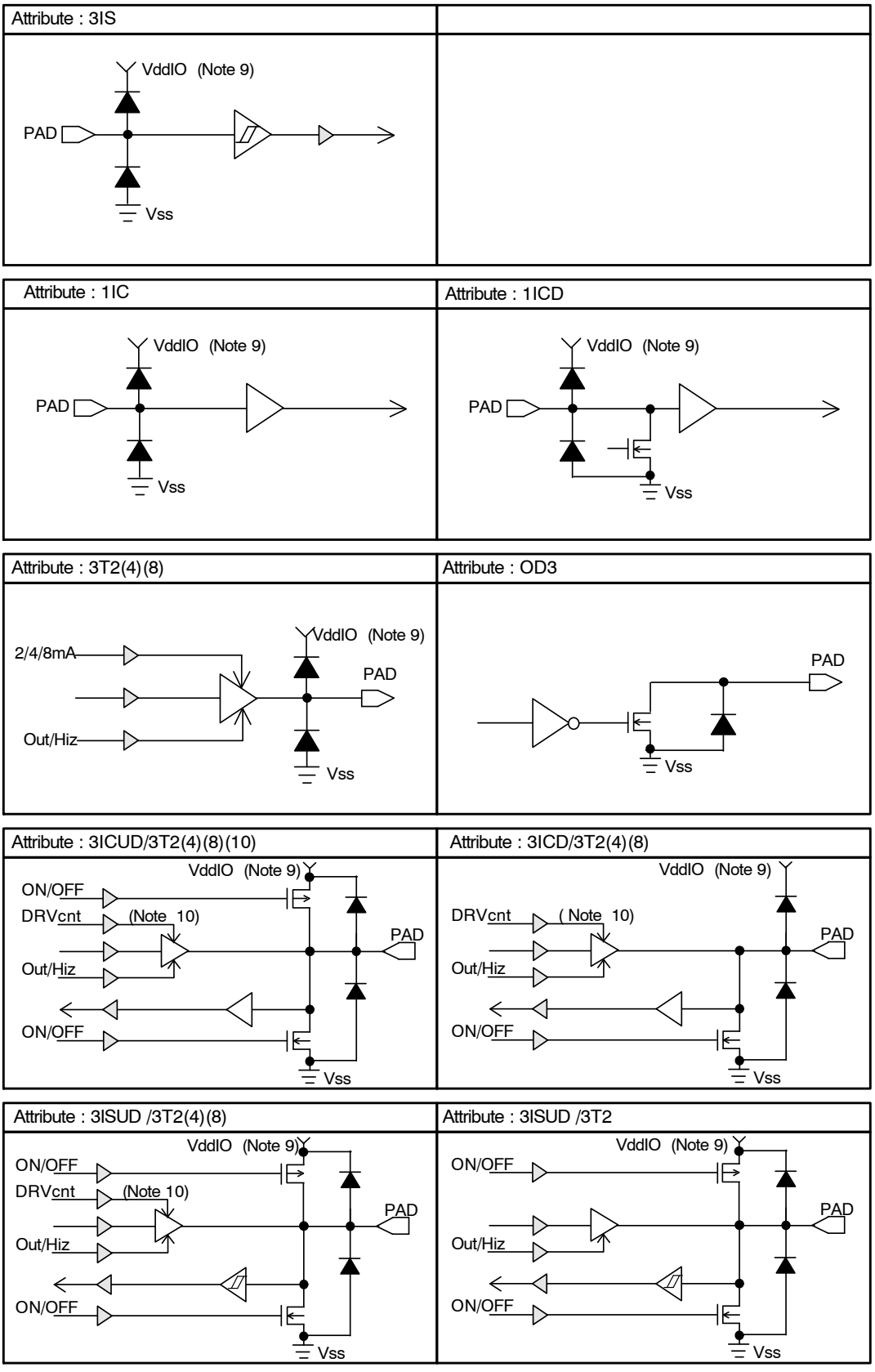
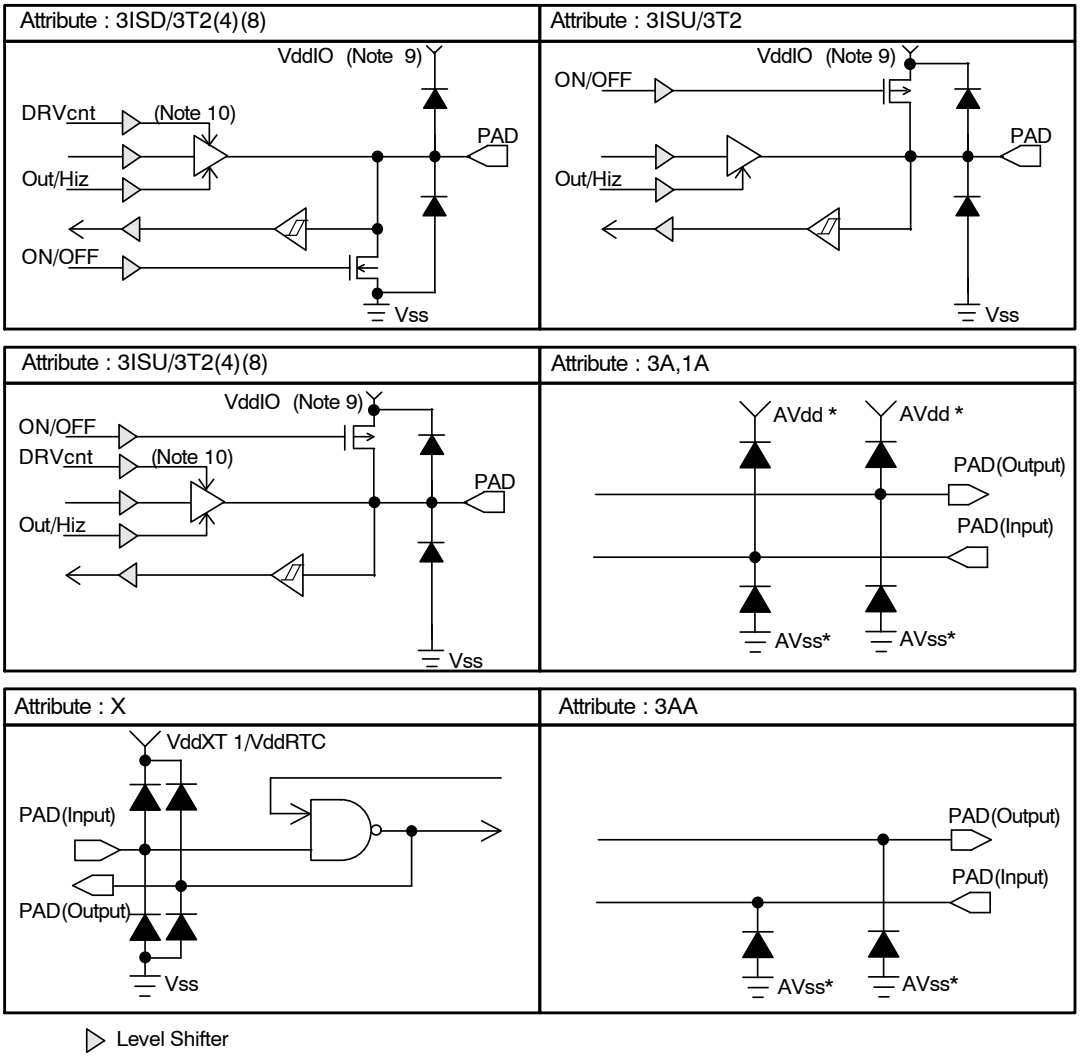


Figure 6. Input/Output Circuit



9. Vdd2, VddSD1 (IO Pwr Grp of Pin Assignment).
10. DRVcnt: 2/4/8 mA, 2/4/8/10 mA, etc. Drivability switch control signal.

Figure 6. Input/Output Circuit (continued)

Table 17. TERMINAL STATE TABLE

TBD 240pin	WLP120	PIN NAME	Default Function (NRES = Low) (Note 11)	Terminal status NRES = Low(i) (Note 12)	Terminal status NRES = High(ii) (Note 12)
•	•	TCLKA0/ BCK1/ GPIO00/ EXTINT00	GPIO00	Hiz	Hiz
•	•	TCLKB0/ LRCK1/ GPIO01/ EXTINT01	GPIO01	Hiz	Hiz
•	•	TIOCB00/ DIN1/ DMDIN0A/ GPIO02/ EXTINT02/	GPIO02	Hiz	Hiz
•	•	TIOCB01/ SFQSCS/ GPIO03/ EXTINT03/ SDCMD0	GPIO03	PU	PU (Note 13)
•	•	TXD1/ SDAT20/ GPIO04/ EXTINT04	GPIO04	Hiz	Hiz
•	•	RXD1/ SDAT21/ GPIO05/ EXTINT05	GPIO05	Hiz	Hiz
•		NCS0/ GPIO06/ EXTINT06	GPIO06	Hiz	Hiz
•	•	SCL0/ GPIO07/ EXTINT07	GPIO07	Hiz	Hiz
•	•	SDA0/ GPIO08/ EXTINT08	GPIO08	Hiz	Hiz
•	•	TIOCA00/ SDCLK2/ PHI0/ GPIO09/ EXTINT09	GPIO09	Hiz	Hiz
•	•	TIOCA01/ SDCMD2/ PHI1/ GPIO0A/ EXTINT0A	GPIO0A	Hiz	Hiz
•	•	TXD2/ TIOCA10/ GPIO0B/ EXTINT0B	GPIO0B	Hiz	Hiz
•	•	RXD2/ TIOCA11/ GPIO0C/ EXTINT0C	GPIO0C	Hiz	Hiz
•	•	SFCK/ GPIO0D/ EXTINT0D/ SDCLK0	GPIO0D	Hiz	Hiz

Table 17. TERMINAL STATE TABLE (continued)

TBD 240pin	WLP120	PIN NAME	Default Function (NRES = Low) (Note 11)	Terminal status NRES = Low(i) (Note 12)	Terminal status NRES = High(ii) (Note 12)
•	•	SDO0/ GPIO1F/ EXTINT1F	GPIO1F	Hiz	Hiz
•	•	TDI/ SDCD1/ SWO/ GPIO20/ EXTINT20	GPIO20	Hiz	Hiz
•	•	TDO/ SDWP1/ GPIO21/ EXTINT21	GPIO21	Hiz	Hiz
•	•	SDCLK1/ GPIO22/ EXTINT22	GPIO22	Hiz	Hiz
•	•	SDCMD1/ GPIO23/ EXTINT23	GPIO23	Hiz	Hiz
•	•	SDAT10/ GPIO24/ EXTINT24	GPIO24	Hiz	Hiz
•	•	SDAT11/ GPIO25/ EXTINT25	GPIO25	Hiz	Hiz
•	•	SDAT12/ GPIO26/ EXTINT26	GPIO26	Hiz	Hiz
•	•	SDAT13/ GPIO27/ EXTINT27	GPIO27	Hiz	Hiz
•	•	TMS/ SDWP2/ GPIO28/ EXTINT28	GPIO28	Hiz	Hiz
•	•	TCK/ SDCD2/ GPIO29/ EXTINT29	GPIO29	Hiz	Hiz
•		SDRADDR12/ GPIO2A/ EXTINT2A	GPIO2A	Hiz	Hiz
•	•	SCL1/ GPIO2B/ EXTINT2B	GPIO2B	Hiz	Hiz
•	•	SDA1/ GPIO2C/ EXTINT2C	GPIO2C	Hiz	Hiz
•	•	SDRADDR11/ DMCKO0A/ GPIO2D/ EXTINT2D	GPIO2D	Hiz	Hiz
•	•	GPIO2E/ EXTINT2E	GPIO2E	Hiz	Hiz
•	•	GPIO2F/ EXTINT2F	GPIO2F	Hiz	Hiz (Note 14)

Table 17. TERMINAL STATE TABLE (continued)

TBD 240pin	WLP120	PIN NAME	Default Function (NRES = Low) (Note 11)	Terminal status NRES = Low(i) (Note 12)	Terminal status NRES = High(ii) (Note 12)
•	•	NWRENWRL/ DIN0/ GPIO30/ EXTINT30	GPIO30	Hiz	Hiz
•	•	NHBNWRH/ TXD0/ DOUT0/ GPIO31/ EXTINT31	GPIO31	Hiz	Hiz
•		EXA1/ GPIO32/ EXTINT32	GPIO32	Hiz	Hiz
•		EXA2/ GPIO33/ EXTINT33	GPIO33	Hiz	Hiz
•		EXA3/ DIN1/ GPIO34/ EXTINT34	GPIO34	Hiz	Hiz
•		EXA4/ DOUT1/ GPIO35/ EXTINT35	GPIO35	Hiz	Hiz
•		EXA5/ GPIO36/ EXTINT36	GPIO36	Hiz	Hiz
•		EXA6/ GPIO37/ EXTINT37	GPIO37	Hiz	Hiz
•		EXA7/ GPIO38/ EXTINT38	GPIO38	Hiz	Hiz
•		EXA8/ GPIO39/ EXTINT39	GPIO39	Hiz	Hiz
•		EXA9/ GPIO3A/ EXTINT3A	GPIO3A	Hiz	Hiz
•		EXA10/ GPIO3B/ EXTINT3B	GPIO3B	Hiz	Hiz
•		EXA11/ GPIO3C/ EXTINT3C	GPIO3C	Hiz	Hiz
•		EXA12/ GPIO3D/ EXTINT3D	GPIO3D	Hiz	Hiz
•		EXA13/ GPIO3E/ EXTINT3E	GPIO3E	Hiz	Hiz
•		EXA14/ GPIO3F/ EXTINT3F	GPIO3F	Hiz	Hiz
•		EXA15/ GPIO40/ EXTINT40	GPIO40	Hiz	Hiz

Table 17. TERMINAL STATE TABLE (continued)

TBD 240pin	WLP120	PIN NAME	Default Function (NRES = Low) (Note 11)	Terminal status NRES = Low(i) (Note 12)	Terminal status NRES = High(ii) (Note 12)
•		EXA16/ GPIO41/ EXTINT41	GPIO41	Hiz	Hiz
•		EXA17/ GPIO42/ EXTINT42	GPIO42	Hiz	Hiz
•		EXA18/ GPIO43/ EXTINT43	GPIO43	Hiz	Hiz
•		EXA19/ GPIO44/ EXTINT44	GPIO44	Hiz	Hiz
•		EXA20/ GPIO45/ EXTINT45	GPIO45	Hiz	Hiz
•		EXD0/ GPIO46/ EXTINT46	GPIO46	Hiz	Hiz
•		EXD1/ GPIO47/ EXTINT47	GPIO47	Hiz	Hiz
•		EXD2/ GPIO48/ EXTINT48	GPIO48	Hiz	Hiz
•		EXD3/ GPIO49/ EXTINT49	GPIO49	Hiz	Hiz
•		EXD4/ GPIO4A/ EXTINT4A	GPIO4A	Hiz	Hiz
•		EXD5/ GPIO4B/ EXTINT4B	GPIO4B	Hiz	Hiz
•		EXD6/ GPIO4C/ EXTINT4C	GPIO4C	Hiz	Hiz
•		EXD7/ GPIO4D/ EXTINT4D	GPIO4D	Hiz	Hiz
•		EXD8/ GPIO4E/ EXTINT4E	GPIO4E	Hiz	Hiz
•		EXD9/ GPIO4F/ EXTINT4F	GPIO4F	Hiz	Hiz
•		EXD10/ GPIO50/ EXTINT50	GPIO50	Hiz	Hiz
•		EXD11/ GPIO51/ EXTINT51	GPIO51	Hiz	Hiz
•		EXD12/ GPIO52/ EXTINT52	GPIO52	Hiz	Hiz

Table 17. TERMINAL STATE TABLE (continued)

TBD 240pin	WLP120	PIN NAME	Default Function (NRES = Low) (Note 11)	Terminal status NRES = Low(i) (Note 12)	Terminal status NRES = High(ii) (Note 12)
•		EXD13/ GPIO53/ EXTINT53	GPIO53	Hiz	Hiz
•		EXD14/ GPIO54/ EXTINT54	GPIO54	Hiz	Hiz
•		EXD15/ GPIO55/ EXTINT55	GPIO55	Hiz	Hiz
•	•	CTS1/ SDAT22/ RXD0/ GPIO56/ EXTINT56	GPIO56	Hiz	Hiz
•	•	RTS1/ SDAT23/ TXD0/ GPIO57/ EXTINT57	GPIO57	Hiz	Hiz
•		PSM_CS	PSM_CS	PD	PD
•		PSM_SDI(DAT0)	PSM_SDI(DAT0)	PD	PD
•		PSM_SDO(DAT1)	PSM_SDO(DAT1)	PD	PD
•		PSM_DAT2	PSM_DAT2	PD	PD
•		PSM_DAT3	PSM_DAT3	PD	PD
•		PSM_SCK	PSM_SCK	PD	PD
•		SDAT00	SDAT00	Hiz	Hiz
•		SDAT01	SDAT01	Hiz	Hiz
•		SDAT02	SDAT02	Hiz	Hiz
•		SDAT03	SDAT03	Hiz	Hiz
•		SDCLK0	SDCLK0	Low	Low
•		SDCMD0	SDCMD0	Hiz	Hiz
•		SDRADDR0	SDRADDR0	Low	Low
•		SDRADDR1	SDRADDR1	Low	Low
•		SDRADDR10	SDRADDR10	Low	Low
•		SDRADDR2	SDRADDR2	Low	Low
•		SDRADDR3	SDRADDR3	Low	Low
•		SDRADDR4	SDRADDR4	Low	Low
•		SDRADDR5	SDRADDR5	Low	Low
•		SDRADDR6	SDRADDR6	Low	Low
•		SDRADDR7	SDRADDR7	Low	Low
•		SDRADDR8	SDRADDR8	Low	Low
•		SDRADDR9	SDRADDR9	Low	Low
•		SDRBA0	SDRBA0	Low	Low
•		SDRBA1	SDRBA1	Low	Low
•		SDRCAS	SDRCAS	High	High
•		SDRCKE	SDRCKE	High	High

Table 17. TERMINAL STATE TABLE (continued)

TBD 240pin	WLP120	PIN NAME	Default Function (NRES = Low) (Note 11)	Terminal status NRES = Low(i) (Note 12)	Terminal status NRES = High(ii) (Note 12)
●		SDRCLK	SDRCLK	Low	Low
●		SDRCS	SDRCS	High	High
●		SDRDATA0	SDRDATA0	Hiz	Hiz
●		SDRDATA1	SDRDATA1	Hiz	Hiz
●		SDRDATA10	SDRDATA10	Hiz	Hiz
●		SDRDATA11	SDRDATA11	Hiz	Hiz
●		SDRDATA12	SDRDATA12	Hiz	Hiz
●		SDRDATA13	SDRDATA13	Hiz	Hiz
●		SDRDATA14	SDRDATA14	Hiz	Hiz
●		SDRDATA15	SDRDATA15	Hiz	Hiz
●		SDRDATA2	SDRDATA2	Hiz	Hiz
●		SDRDATA3	SDRDATA3	Hiz	Hiz
●		SDRDATA4	SDRDATA4	Hiz	Hiz
●		SDRDATA5	SDRDATA5	Hiz	Hiz
●		SDRDATA6	SDRDATA6	Hiz	Hiz
●		SDRDATA7	SDRDATA7	Hiz	Hiz
●		SDRDATA8	SDRDATA8	Hiz	Hiz
●		SDRDATA9	SDRDATA9	Hiz	Hiz
●		SDRDQM0	SDRDQM0	High	High
●		SDRDQM1	SDRDQM1	High	High
●		SDRRAS	SDRRAS	High	High
●		SDRWE	SDRWE	High	High
●	●	SWDCLK/ DMCKO0B/ GPIO58/ EXTINT58	SWDCLK	Hiz	Hiz
●	●	SWDIO/ DMDIN0B/ GPIO59/ EXTINT59	SWDIO	Hiz	Hiz
●	●	NRES	NRES	Hiz	Hiz
●	●	TEST	TEST	Hiz	Hiz
●		XTALINFO0	XTALINFO0	Hiz	Hiz
●		XTALINFO1	XTALINFO1	Hiz	Hiz
●	●	BMODE0	BMODE0	Hiz	Hiz
●	●	BMODE1	BMODE1	Hiz	Hiz
●	●	IO18V	IO18V	Hiz	Hiz
●		RTCMODE	RTCMODE	Hiz	Hiz
●	●	KEYINT0	KEYINT0	PD	PD
●	●	USBDM	USBDM	Low	Low
●	●	KEYINT1	KEYINT1	PD	PD
●		KEYINT2	KEYINT2	PD	PD
●		BACKUPB	BACKUPB	Hiz	Hiz

Table 17. TERMINAL STATE TABLE (continued)

TBD 240pin	WLP120	PIN NAME	Default Function (NRES = Low) (Note 11)	Terminal status NRES = Low(i) (Note 12)	Terminal status NRES = High(ii) (Note 12)
●	●	RTCINT	RTCINT	−(Not Determined)	−(Not Determined)
●	●	VDET	VDET	Hiz	Hiz
●	●	LOUT/ GPLOUT	LOUT	Hiz	Hiz
●	●	ROUT/ GPROUT	ROUT	Hiz	Hiz
●	●	USBDP	USBDP	Low	Low
●	●	USBID	USBID	Hiz	Hiz
●	●	USBEXT02	USBEXT02	−(Not Applicable)	−(Not Applicable)
●	●	USBVBUS	USBVBUS	Hiz	Hiz
●		VCNT1	VCNT1	−(Not Applicable)	−(Not Applicable)
●		VCNT2	VCNT2	−(Not Applicable)	−(Not Applicable)
●	●	SIN0	SIN0	−(Not Applicable)	−(Not Applicable)
●	●	SIN1	SIN1	−(Not Applicable)	−(Not Applicable)
●	●	SIN2	SIN2	−(Not Applicable)	−(Not Applicable)
●		SIN3	SIN3	−(Not Applicable)	−(Not Applicable)
●		SIN4	SIN4	−(Not Applicable)	−(Not Applicable)
●		SIN5	SIN5	−(Not Applicable)	−(Not Applicable)
●		SIN6	SIN6	−(Not Applicable)	−(Not Applicable)
●		SIN7	SIN7	−(Not Applicable)	−(Not Applicable)
●	●	XIN1	XIN1	−(Not Applicable)	−(Not Applicable)
●	●	XIN32K	XIN32K	−(Not Applicable)	−(Not Applicable)
●	●	XOUT1	XOUT1	−(Not Applicable)	−(Not Applicable)
●	●	XOUT32K	XOUT32K	−(Not Applicable)	−(Not Applicable)

*"●" Means a port is available for each package. "PD" means pull down.
11. Default function is port function set by NRES = Low.
12. NRES = High(ii) occurs just after NRES = Low(i).
13. This terminal is configured as an output terminal with PU disabled, and used as QSCS for the SPI I/F chip select during serial flash boot mode.
14. This terminal is configured as an output terminal and used as the boot monitor port during Internal ROM boot.

ELECTRICAL SPECIFICATION

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 18. MAXIMUM RATINGS (*VSS* = 0V)

Item	Symbol	Condition	Ratings	Unit
Maximum power supply voltage	Vdd1 VddXT1 AVddPLL1 AVddPLL2 VddRTC		−0.3 to 1.2	V
	DVddUSBPHY1		−0.3 to 1.2	V
	AVddADC AVddUSBPHY18 AVddDAMPL AVddDAMPR		−0.3 to 2.0	V
	Vdd2 VddSD1 AVddUSBPHY2		−0.3 to 3.65	V
Input voltage	VI		−0.3 to *Vdd*+0.3	V
	VIUSB1	USBDP,USBDM terminal	−0.3 to 6.0	V
	VIUSB2	USBVBUS terminal	−0.3 to 6.0	V
Operating ambient temperature	Topr		−20 to +65	°C
Ambient temperature of preservation	Tstg		−55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 19. RECOMMENDATION OPERATING CONDITIONS (T_A = −20°C to +65°C)

Item	Symbol	Condition	Low voltage operation (Note 15)			High voltage operation (Note 15)			Unit
			Min	Typ	Max	Min	Typ	Max	
Power supply voltage	Vdd1		0.95	1.0	1.155	1.05	1.1	1.155	V
	VddXT1		0.95	1.0	1.155	same as left			V
	AVddPLL1		0.95	1.0	1.155	same as left			V
	AVddPLL2		0.95	1.0	1.155	same as left			V
	VddRTC	(Note 16)	0.765		0.90	same as left			V
			0.90	1.0	1.155	same as left			V
	Vdd2	(Note 17)	2.7	3.3	3.6	same as left			V
		(Note 17)	1.7	1.8	1.95	same as left			V
	VddSD1	(Note 18)	2.7	3.3	3.6	same as left			V
		(Note 18)	1.7	1.8	1.95	same as left			V
	AVddADC		1.7	1.8	1.95	same as left			V
	DVddUSBPHY1	(Note 19)	0.93	1.0	1.1	same as left			V
		(Note 20)	0.93	1.0	1.155	same as left			V
	AVddUSBPHY2	(Note 19)	3.07	3.3	3.6	same as left			V
		(Note 20)	2.7	3.3	3.6	same as left			V
	AVddUSBPHY18	(Note 19)	1.7	1.8	1.95	same as left			V
		(Note 20)	1.7	1.8	1.95	same as left			V
	AVddDAMPL		0.95	1.5	1.65	same as left			V
		(Note 21)	0.95	1.5	1.95	same as left			V
	AVddDAMPR		0.95	1.5	1.65	same as left			V
		(Note 21)	0.95	1.5	1.95	same as left			V
Input range	VIN		0		*Vdd*	same as left			V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

15. Follow the operating frequency specifications because the operating frequency ranges are specified according to the operating voltage ranges.
16. APB clock needs 57.5 MHz or less.
17. IO terminals operating at Vdd2 need to be specified for the IO voltage range of either 3.3 V or 1.8 V according to the Vdd2 voltage by using the IO18 V terminal. When setting 1.8 V IO interface, even for extremely short period, don't supply not only the 3.3 V voltage range but also any voltage over the 1.8 V voltage range to Vdd2.
18. IO terminals operating at VddSD1 need to be specified for the IO voltage range of either 3.3V or 1.8V according to the VddSD1 voltage by setting a register "System Controller" described in the "System Functions User's Manual". When setting 1.8 V IO interface, even for extremely short period, don't supply not only the 3.3 V voltage range but also any voltage over the 1.8 V voltage range to VddSD1.
19. While USB is used (including USB suspend mode).
20. While USB is not used.
21. While used as GPO (general purpose output) the output of which can be controlled by registers.

The power domains of Vdd1, DVddUSBPHY1, AVddPLL1, AVddPLL2, VddXT1 are divided, and different voltages can be supplied.
The power domains of Vdd2, VddSD1, AVddADC, AVddUSBPHY2, AVdd USBPHY18, AvddDAMPL = AVddDAMPR are divided, and difference voltages can be supplied.
If power is supplied to one of the power supply pins above, all the other power supply pins should also be supplied.
However, DVddUSBPHY1, AVddUSBPHY18 and AVddUSBPHY2 can all be turned off to reduce leakage current while USB is not used. In addition, VddRTC can be supplied if BACKUPB is set to low, while other power supply pins are not supplied.

Table 20. RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Function	Low voltage operation			High voltageoperation			Unit
			Min	Typ	Max	Min	Typ	Max	
Xtal Input frequency	Fxin1	System, Audio clock (XT1 oscillator)	12 MHz or 19.2 MHz or 24 MHz Tolerance: ±50 ppm or less			same as left			–
	FxinRTC	RTC clock (XTRTC oscillator)	32.768 kHz Tolerance : ±50ppm or less			same as left			–
	Frc	RC (RC oscillator)	0.4 (Note 25)	1 (Note 25)	2 (Note 25)	same as left			MHz
Time for Xtal stable	Txin1				3 (Note 26)	same as left			ms
	TxinRTC				1000 (Note 26)	same as left			ms
Internal clock frequency	Farm	Cortex−M3	0		115	0		170	MHz
	Fahb	AHB	0		115	0		170	MHz
	Fapb	APB	0		115	0		170	MHz
	Fdsp	DSP	0		115	0		170	MHz
	Faud (Note 22)	AUDCLK(768fs)	0	33.8688	147.456	same as left			MHz
	Fdec	DECCLK (Note 23) (MP3 Decoder)	0	16.9344	73.728	same as left			MHz
	Fenc	ENCCLK (Note 24) (MP3 Encoder)	0	8.4672	36.864	same as left			MHz

22. Audio blocks run on a clock of 256 * Fs(sampling frequency).
    However, Class−D AMP, etc. run at 384 * Fs(sampling frequency).
    These clocks are generated from 768 * Fs(Base Clock) divided by 3 and 2 respectively.
23. MP3 Decoder runs on a clock of 384 * Fs(sampling frequency of MPEG1 mode).
    It runs on the clock of the same frequency as MPEG1 mode during MPEG2 / 2.5 mode. For example, even when operating in MPEG2 / 2.5 mode(Fs = 22.05 / 11.025 KHz as an example), please supply 16.9344MHz(= 384 * 44.1 KHz) clock which is the same clock frequency as MPEG1 mode.
24. MP3 Encoder runs on a clock of 192 * Fs(sampling frequency of MPEG1 mode).
    It runs on the clock of the same frequency as MPEG1 mode during MPEG2 / 2.5 mode. For example, even when operating in MPEG2 / 2.5 mode(Fs = 22.05 / 11.025 KHz as an example), please supply 8.4672Mhz (= 192 * 44.1 KHz) clock which is the same clock frequency as MPEG1 mode.
25. Vdd1 = 0.95 V to 1.155 V, Ta = −25°C to +65°C.
26. It is a reference level in Ta = 25°C. Adjustment is necessary by the situation of the set.

Table 21. DC CHARACTERISTICS

(Vdd2 = 2.7 V to 3.6 V, VddSD1 = 2.7 V to 3.6 V, VddRTC = 0.765 V to 1.155 V, Ta = −20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Input H voltage	V_{IH}	(1)(2)(4)	CMOS	0.7 x Vdd2			V
		(3)		0.7 x VddSD1			V
		(6)(8)	Schmitt	0.75 x Vdd2			V
		(7)		0.75 x VddSD1			V
		(5)(9)	CMOS	0.7 x VddRTC			V
Input L voltage	V_{IL}	(1)(2)(4)	CMOS			0.25 x Vdd2	V
		(3)				0.25 x VddSD1	V
		(6)(8)	Schmitt			0.2 x Vdd2	V
		(7)				0.2 x VddSD1	V
		(5)(9)	CMOS			0.2 x VddRTC	V
Output H voltage	V_{OH}	(10)(11)(12) (14)(15)(17)	I_{OH} = −2 mA	Vdd2 − 0.4			V
		(13)(16)		VddSD1 − 0.4			V
		(10) (14)(15)(17)	I_{OH} = −4 mA	Vdd2 − 0.4			V
		(16)		VddSD1 − 0.4			V
		(10) (14)(15)(17)	I_{OH} = −8 mA	Vdd2 − 0.4			V
		(16)		VddSD1 − 0.4			V
		(14)(15)(17)	I_{OH} = −10 mA	Vdd2 − 0.4			V
		(16)		VddSD1 − 0.4			V
Output L voltage	V_{OL}	(10)(11)(12) (14)(15)(17)	I_{OL} = 2 mA			0.4	V
		(13)(16)				0.4	V
		(10) (14)(15)(17)	I_{OL} = 4 mA			0.4	V
		(16)				0.4	V
		(10) (14)(15)(17)	I_{OL}= 8 mA			0.4	V
		(16)				0.4	V
		(14)(15)(17)	I_{OL} = 10 mA			0.4	V
		(16)				0.4	V
		(18)	I_{OL} = 0.3 mA			0.3	V
Pull−up resistor	Rup	(20)(21)		30		150	kΩ
		(22)		25		80	kΩ
		(23)		18		50	kΩ
Pull−down resistor	Rdn	(19)(21)		30		150	kΩ
		(22)		25		80	kΩ
		(23)		18		50	kΩ
Input leak current	I_{IL}	(1)(2)(3) (4)(5)(6) (7)(8)(9)	VI = Vdd* = Vss	−10		10	μA
Output leak current	I_{OZ}	(10)(11)(12) (13)(14)(15) (16)(17)(18)	HiZ output	−10		10	μA

Table 22. DC CHARACTERISTICS

(Vdd2 = 1.7 V to 1.95 V, VddSD1 = 1.7 V to 1.95 V, AVddDAMPL = 0.95 V to 1.95 V, AVddDAMPR = 0.95 V to 1.95 V, Ta = −20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Input H voltage	V_{IH}	(1)(2)(4)	CMOS	0.7 x Vdd2			V
		(3)		0.7 x VddSD1			V
		(6)(8)	Schmitt	0.75 x Vdd2			V
		(7)		0.75 x VddSD1			V
Input L voltage	V_{IL}	(1)(2)(4)	CMOS			0.3 x Vdd2	V
		(3)				0.3 x VddSD1	V
		(6)(8)	Schmitt			0.25 x Vdd2	V
		(7)				0.25 x VddSD1	V
Output H voltage	V_{OH}	(10)(11)(12) (14)(15)(17)	I_{OH} = −2 mA	Vdd2 − 0.4			V
		(13)(16)		VddSD1 − 0.4			V
		(10) (14)(15)(17)	I_{OH} = −4 mA	Vdd2 − 0.4			V
		(16)		VddSD1 − 0.4			V
		(14)(15)(17)	I_{OH} = −8 mA	Vdd2 − 0.4			V
		(16)		VddSD1 − 0.4			V
		(14)(15)(17)	I_{OH} = −10 mA	Vdd2 − 0.4			V
		(16)		VddSD1 − 0.4			V
		(24)	I_{OH} = −8 mA (Note 27)	AVddDAMPL − 0.4			V
		(25)	I_{OH} = −8 mA (Note 27)	AVddDAMPR − 0.4			V
Output L voltage	V_{OL}	(10)(11)(12) (14)(15)(17)	I_{OL} = 2 mA			0.4	V
		(13)(16)				0.4	V
		(10) (14)(15)(17)	I_{OL} = 4 mA			0.4	V
		(16)				0.4	V
		(10) (14)(15)(17)	I_{OL} = 8 mA			0.4	V
		(16)				0.4	V
		(14)(15)(17)	I_{OL} = 10 mA			0.4	V
		(16)				0.4	V
		(24)	I_{OL} = 8 mA			0.4	V
		(25)	I_{OL} = 8 mA			0.4	V
Pull−up resistor	Rup	(20)(21)		30		200	kΩ
		(22)		25		80	kΩ
		(23)		18		50	kΩ
Pull−down resistor	Rdn	(19)(21)		30		200	kΩ
		(22)		25		80	kΩ
		(23)		18		50	kΩ
Input leak current	I_{IL}	(1)(2)(3) (4)(5)(6) (7)(8)(9)	VI = Vdd* = Vss	−10		10	μA
Output leak current	I_{OZ}	(10)(11)(12) (13)(14)(15) (16)(17)	HiZ output	−10		10	μA
		(24)(25)		−10		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

(1) SDRDATA15, SDRDATA14, SDRDATA13, SDRDATA12, SDRDATA11, SDRDATA10, SDRDATA9, SDRDATA8, SDRDATA7, SDRDATA6, SDRDATA5, SDRDATA4, SDRDATA3, SDRDATA2, SDRDATA1, SDRDATA0

(2) SDCLK2(GPIO09), SDCMD2(GPIO0A), SDAT23(GPIO57), SDAT22(GPIO56), SDAT21(GPIO05), SDAT20(GPIO04), PSM_SCK, PSM_CS, PSM_SDI, PSM_SDO, PSM_DAT2, PSM_DAT3
(3) SDCLK1(GPIO22), SDCMD1(GPIO23), SDAT13(GPIO27), SDAT12(GPIO26), SDAT11(GPIO25), SDAT10(GPIO24)
(4) SDCMD0, SDAT03, SDAT02, SDAT01, SDAT00, SFCK(GPIO0D), SFDI(GPIO0E), SFDO(GPIO0F), SFWP(GPIO11), SFHOLD(GPIO12), TIOCB01(GPIO03)
(5) RTCMODE, VDET
(6) SDWP2(GPIO28), SDCD2(GPIO29), EXD0(GPIO46), EXD1(GPIO47), EXD2(GPIO48), EXD3(GPIO49), EXD4(GPIO4A), EXD5(GPIO4B), EXD6(GPIO4C), EXD7(GPIO4D), EXD8(GPIO4E), EXD9(GPIO4F), EXD10(GPIO50), EXD11(GPIO51), EXD12(GPIO52), EXD13(GPIO53), EXD14(GPIO54), EXD15(GPIO55), EXA1(GPIO32), EXA2(GPIO33), EXA3(GPIO34), EXA4(GPIO35), EXA5(GPIO36), EXA6(GPIO37), EXA7(GPIO38), EXA8(GPIO39), EXA9(GPIO3A), EXA10(GPIO3B), EXA11(GPIO3C), EXA12(GPIO3D), EXA13(GPIO3E), EXA14(GPIO3F), EXA15(GPIO40), EXA16(GPIO41), EXA17(GPIO42), EXA18(GPIO43), EXA19(GPIO44), EXA20(GPIO45), NRD(GPIO17), NLBEXA0(GPIO16), NHBNWRH(GPIO31), NCS1(GPIO10), NCS0(GPIO06), NWRENWRL(GPIO30), SWDIO(GPIO59), DOUT1(GPIO15), BCK1(GPIO13), MCLK0(GPIO18), LRCK1(GPIO14), BCK0(GPIO19), LRCK0(GPIO1A), DIN0(GPIO1B), XTALINFO1, DOUT0(GPIO1C), NRES, SCL1(GPIO2B), SDA1(GPIO2C), TCLKA0(GPIO00), TCLKB0(GPIO01), EXTINT2E(GPIO2E), EXTINT2F(GPIO2F), TXD2(GPIO0B), RXD2(GPIO0C), TIOCB00(GPIO02), XTALINFO0, SDO0(GPIO1F), SCK0(GPIO1D), SCL0(GPIO07), SDI0(GPIO1E), SDA0(GPIO08), SWDCLK(GPIO58), SDRADDR12(GPIO2A), SDRADDR11(GPIO2D)
(7) SDWP1(GPIO21), SDCD1(GPIO20)
(8) BMODE0, BMODE1
(9) Keyint2, Keyint0, Keyint1, BACKUPB, TEST
(10) EXD0(GPIO46), EXD1(GPIO47), EXD2(GPIO48), EXD3(GPIO49), EXD4(GPIO4A), EXD5(GPIO4B), EXD6(GPIO4C), EXD7(GPIO4D), EXD8(GPIO4E), EXD9(GPIO4F), EXD10(GPIO50), EXD11(GPIO51), EXD12(GPIO52), EXD13(GPIO53), EXD14(GPIO54), EXD15(GPIO55), EXA1(GPIO32), EXA2(GPIO33), EXA3(GPIO34), EXA4(GPIO35), EXA5(GPIO36), EXA6(GPIO37), EXA7(GPIO38), EXA8(GPIO39), EXA9(GPIO3A), EXA10(GPIO3B), EXA11(GPIO3C), EXA12(GPIO3D), EXA13(GPIO3E), EXA14(GPIO3F), EXA15(GPIO40), EXA16(GPIO41), EXA17(GPIO42), EXA18(GPIO43), EXA19(GPIO44), EXA20(GPIO45), NRD(GPIO17), NLBEXA0(GPIO16), NHBNWRH(GPIO31), NCS1(GPIO10), NCS0(GPIO06), NWRENWRL(GPIO30), DOUT1(GPIO15), BCK1(GPIO13), MCLK0(GPIO18), LRCK1(GPIO14), BCK0(GPIO19), LRCK0(GPIO1A), DIN0(GPIO1B), XTALINFO1, DOUT0(GPIO1C), SCL1(GPIO2B), SDA1(GPIO2C), TCLKA0(GPIO00), TCLKB0(GPIO01), EXTINT2E(GPIO2E), EXTINT2F(GPIO2F), TXD2(GPIO0B), RXD2(GPIO0C), TIOCB00(GPIO02), XTALINFO0, SDO0(GPIO1F), SCK0(GPIO1D), SCL0(GPIO07), SDI0(GPIO1E), SDA0(GPIO08), SWDCLK(GPIO58), SDRADDR0, SDRADDR1, SDRADDR2, SDRADDR3, SDRADDR4, SDRADDR5, SDRADDR6, SDRADDR7, SDRADDR8, SDRADDR9, SDRADDR10, SDRADDR11(GPIO2D), SDRADDR12(GPIO2A), SDRDATA0, SDRDATA1, SDRDATA2, SDRDATA3, SDRDATA4, SDRDATA5, SDRDATA6, SDRDATA7, SDRDATA8, SDRDATA9, SDRDATA10, SDRDATA11, SDRDATA12, SDRDATA13, SDRDATA14, SDRDATA15, SDRBA1, SDRBA0, SDRCKE, SDRCS, SDRWE, SDRCAS, SDRRAS, SDRDQM1, SDRDQM0, SDWP2(GPIO28), SDCD2(GPIO29)
(11) SWDIO(GPIO59)
(12) BMODE0, BMODE1
(13) SDWP1(GPIO21), SDCD1(GPIO20)
(14) SDCLK0, SDCMD0, SDAT03, SDAT02, SDAT01, SDAT00, SFCK(GPIO0D), SFDI(GPIO0E), SFDO(GPIO0F), SFWP(GPIO11), SFHOLD(GPIO12), TIOCB01(GPIO03)
(15) SDCLK2(GPIO09), SDCMD2(GPIO0A), SDAT23(GPIO57), SDAT22(GPIO56), SDAT21(GPIO05), SDAT20(GPIO04), PSM_SCK, PSM_CS, PSM_SDI, PSM_SDO, PSM_DAT2, PSM_DAT3
(16) SDCLK1(GPIO22), SDCMD1(GPIO23), SDAT13(GPIO27), SDAT12(GPIO26), SDAT11(GPIO25), SDAT10(GPIO24),
(17) SDRCLK
(18) RTCINT
(19) EXD0(GPIO46), EXD1(GPIO47), EXD2(GPIO48), EXD3(GPIO49), EXD4(GPIO4A), EXD5(GPIO4B), EXD6(GPIO4C), EXD7(GPIO4D), EXD8(GPIO4E), EXD9(GPIO4F), EXD10(GPIO50), EXD11(GPIO51), EXD12(GPIO52), EXD13(GPIO53), EXD14(GPIO54), EXD15(GPIO55), EXA1(GPIO32), EXA2(GPIO33), EXA3(GPIO34), EXA4(GPIO35), EXA5(GPIO36), EXA6(GPIO37), EXA7(GPIO38), EXA8(GPIO39), EXA9(GPIO3A), EXA10(GPIO3B), EXA11(GPIO3C), EXA12(GPIO3D), EXA13(GPIO3E), EXA14(GPIO3F), EXA15(GPIO40), EXA16(GPIO41), EXA17(GPIO42), EXA18(GPIO43), EXA19(GPIO44), EXA20(GPIO45), NRD(GPIO17), NLBEXA0(GPIO16), NHBNWRH(GPIO31), NWRENWRL(GPIO30), SDRDATA0, SDRDATA1, SDRDATA2, SDRDATA3, SDRDATA4, SDRDATA5, SDRDATA6, SDRDATA7, SDRDATA8, SDRDATA9, SDRDATA10, SDRDATA11, SDRDATA12, SDRDATA13, SDRDATA14, SDRDATA15, Keyint0, Keyint1, Keyint2
(20) NCS1(GPIO10), NCS0(GPIO06), XTALINFO1, XTALINFO0, SWDIO(GPIO59)
(21) DOUT1(GPIO15), BCK1(GPIO13), MCLK0(GPIO18), LRCK1(GPIO14), BCK0(GPIO19), LRCK0(GPIO1A), DIN0(GPIO1B), DOUT0(GPIO1C), SCL1(GPIO2B), SDA1(GPIO2C), TCLKA0(GPIO00), TCLKB0(GPIO01), SDO0(GPIO1F), SCK0(GPIO1D), SCL0(GPIO07), SDI0(GPIO1E), SDA0(GPIO08), EXTINT2E(GPIO2E), EXTINT2F(GPIO2F), TXD2(GPIO0B), RXD2(GPIO0C), TIOCB00(GPIO02), SWDCLK(GPIO58), SDWP1(GPIO21), SDCD1(GPIO20), SDRADDR11(GPIO2D), SDRADDR12(GPIO2A), SDWP2(GPIO28), SDCD2(GPIO29)
(22) SDCLK1(GPIO22), SDCMD1(GPIO23), SDAT13(GPIO27), SDAT12(GPIO26), SDAT11(GPIO25), SDAT10(GPIO24), SDCLK2(GPIO09), SDCMD2(GPIO0A), SDAT23(GPIO57), SDAT22(GPIO56), SDAT21(GPIO05), SDAT20(GPIO04), PSM_SCK, PSM_CS, PSM_SDI, PSM_SDO, PSM_DAT2, PSM_DAT3, BMODE0, BMODE1
(23) SDCMD0, SDAT03, SDAT02, SDAT01, SDAT00, SFCK(GPIO0D), SFDI(GPIO0E), SFDO(GPIO0F), SFWP(GPIO11), SFHOLD(GPIO12), TIOCB01(GPIO03)
(24) LOUT(used as GPLOUT)
(25) ROUT(used as GPROUT)

27. Set DAMPCTL register as below.
– DZCTL: DSLEEP = 1. (don't care DSL value)
- DZINP: DZINP13 = 1, other DZINPx = 0
This DC characteristics can be applied while Class−D AMP used as GPO.

PLL Characteristics

PLL1 (System)

Table 23. PLL1 (SYSTEM)

Vdd1 (Note 28) = 0.95 to 1.155 V, AVddPLL1 (Note 28) = 0.95 to 1.155 V, T_A = −20°C to +65°C

Item	Symbol	Condition	Min	Typ	Max	Unit
VCO control voltage	VCNT1		0		AVddPLL1	V
VCO highest oscillation frequency	Fmax		400			MHz
VCO lowest oscillation frequency	Fmin				100	MHz
Phase comparison frequency (Note 29)	Fref				10	MHz
PLL lock time (Note 29)	Tlock1 (Note 30)	Internal loop filter Fref = 1.0 MHz, 1.2 MHz			0.61	ms
	Tlock2 (Note 30)	External loop filter Fref = 1.0 MHz, 1.2 MHz			1.25	ms
Jitter (Note 29)	Jitter	VCO frequency = 400 MHz		±5.94	±10.1	%

28. Power up and power down timing of AVddPLL1 and Vdd1 should be as close as possible.
29. Electrical specifications are based on simulation results.
30. PLL lock time and appropriate LPF circuit depend on phase comparison frequency (Fref).

Table 24. PLL1 SETTING FOR XT1 OSCILLATION

XT1 Frequency [MHz]	VCO Frequency [MHz]	PLL1 Divide M	PLL1 Multiply N	Phase Comparison Frequency Fref [MHz]
12	100 to 400	12	100 to 400	1.0
19.2	100.8 to 399.6	16	84 to 333	1.2
24	100 to 400	24	100 to 400	1.0

Table 25. LOOP FILTER FOR PLL1

Loop filter	Xtal Oscillation, Fref	PLL1 multiply N		S3 (Note 31)	S2 (Note 31)	S1 (Note 31)	S0 (Note 31)	R1[kΩ] (Note 31)	R2[kΩ] (Note 31)	C1[pF] (Note 31)	C2[pF] (Note 31)
		min	max					typ	typ	typ	typ
Internal	XT1 = 12 MHz, Fref = 1.0 MHz XT1 = 19.2 MHz, Fref = 1.2 MHz XT1 = 24 MHz, Fref = 1.0 MHz	1440	-	1	1	1	1	–	–	–	–
		1008	1439	1	1	1	0				
		698	1007	1	1	0	1				
		485	697	1	1	0	0				
		338	484	1	0	1	1				
		234	337	1	0	1	0				
		163	233	1	0	0	1				
		114	162	1	0	0	0				
		80	113	0	1	1	1				
		55	79	0	1	1	0				
		38	54	0	1	0	1				
		27	37	0	1	0	0				
		19	26	0	0	1	1				
		13	18	0	0	1	0				
		9	12	0	0	0	1				
		-	8	0	0	0	0				
External	XT1 = 12 MHz, Fref = 1.0 MHz XT1 = 19.2 MHz, Fref = 1.2 MHz XT1 = 24 MHz, Fref = 1.0 MHz	–						–	6.8 (Note 32)	330 (Note 32)	3300 (Note 32)

31. Regarding internal loop filter use, appropriate loop filter parameters need to be selected according to PLL1 multiply N value. Regarding external loop filter use, the loop filter parameters need to be attached externally.
32. Each value must be supplied by external resistor and capacitor. Refer to PLL1 (System) in Application.

Audio PLL

Table 26. AUDIO PLL

Vdd1 (Note 33) = 0.95 to 1.155 V, AVddPLL2 (Note 33) = 0.95 to 1.155 V, T_A = −20°C to +65°C

Item	Symbol	Condition	Min	Typ	Max	Unit
VCO control voltage	VCNT2		0		AVddPLL2	V
VCO highest oscillation frequency	Fmax		150			MHz
VCO lowest oscillation frequency	Fmin				95	MHz
Phase comparison frequency (Note 34)	Fref				10	MHz
PLL lock time (Note 34)	Tlock1 (Note 35)	Internal loop filter Fref = 96 KHz, 19.2 KHz, 768 KHz, 153.6 KHz, 192 KHz, 38.4 KHz			15.4	ms
	Tlock2 (Note 35)	External loop filter Fref = 96 KHz, 19.2 KHz, 768 KHz, 153.6 KHz, 192 KHz, 38.4 KHz			7.7	ms
Jitter (Note 34)	Jitter1	VCO frequency = 98.304 MHz		±2.88	±4.9	%
	Jitter2	VCO frequency = 135.4752 MHz		±3.41	±5.8	%
	Jitter3	VCO frequency = 147.456 MHz		±3.59	±6.1	%

33. Power up and power down timing of AVddPLL2 and Vdd1 should be as close as possible.
34. Electrical specifications are based on simulation results.
35. PLL lock time and appropriate LPF circuit depend on phase comparison frequency (Fref).

Table 27. PLL2 SETTING FOR XT1 OSCILLATION

XT1 Frequency [MHz]	VCO Frequency [MHz] (Note 36)	Sampling Frequency Fs	PLL2 Divide M	PLL2 Multiply N	Phase Comparison Frequency Fref [KHz]
12	98.304	8 KHz	125	1024	96
		16 KHz			
		32 KHz			
		64 KHz			
		128 KHz			
	135.4752	11.025 KHz	625	7056	19.2
		22.05 KHz			
		44.1 KHz			
		88.2 KHz			
		176.4 KHZ			
	147.456	12 KHz	125	1536	96
		24 KHZ			
		48 KHz			
		96 KHz			
		192 KHz			

Table 27. PLL2 SETTING FOR XT1 OSCILLATION (continued)

XT1 Frequency [MHz]	VCO Frequency [MHz] (Note 36)	Sampling Frequency Fs	PLL2 Divide M	PLL2 Multiply N	Phase Comparison Frequency Fref [KHz]
19.2	98.304	8 KHz	25	128	768
		16 KHz			
		32 KHz			
		64 KHz			
		128 KHz			
	135.4752	11.025 KHz	125	882	153.6
		22.05 KHz			
		44.1 KHz			
		88.2 KHz			
		176.4 KHZ			
	147.456	12 KHz	25	192	768
		24 KHZ			
		48 KHz			
		96 KHz			
		192 KHz			
24	98.304	8 KHz	125	512	192
		16 KHz			
		32 KHz			
		64 KHz			
		128 KHz			
	135.4752	11.025 KHz	625	3528	38.4
		22.05 KHz			
		44.1 KHz			
		88.2 KHz			
		176.4 KHZ			
	147.456	12 KHz	125	768	192
		24 KHZ			
		48 KHz			
		96 KHz			
		192 KHz			

36. VCO frequency = 768×Fs×n (n = 16, 8, 4, 2, and 1)

Table 28. PLL2 SETTING FOR BCLK

BCLK Frequency [MHz]		VCO Frequency [MHz] (Note 37)	Sampling Frequency Fs	PLL2 Divide M	PLL2 Multiply N	Phase Comparison Frequency Fref [KHz]
32Fs	0.256	98.304	8 KHz	1	384	256
	0.512		16 KHz	2		
	1.024		32 KHz	4		
	2.048		64 KHz	8		
	4.096		128 KHz	16		
	0.3528	135.4752	11.025 KHz	1	384	352.8
	0.7056		22.05 KHz	2		
	1.4112		44.1 KHz	4		
	2.8224		88.2 KHz	8		
	5.6448		176.4 KHZ	16		
	0.384	147.456	12 KHz	1	384	384
	0.768		24 KHZ	2		
	1.536		48 KHz	4		
	3.072		96 KHz	8		
	6.144		192 KHz	16		
48Fs	0.384	98.304	8 KHz	1	256	384
	0.768		16 KHz	2		
	1.536		32 KHz	4		
	3.072		64 KHz	8		
	6.144		128 KHz	16		
	0.5292	135.4752	11.025 KHz	2	512	264.6
	1.0584		22.05 KHz	4		
	2.1168		44.1 KHz	8		
	4.2336		88.2 KHz	16		
	8.4672		176.4 KHZ	32		
	0.576	147.456	12 KHz	2	512	288
	1.152		24 KHZ	4		
	2.304		48 KHz	8		
	4.608		96 KHz	16		
	9.216		192 KHz	32		

Table 28. PLL2 SETTING FOR BCLK (continued)

BCLK Frequency [MHz]		VCO Frequency [MHz] (Note 37)	Sampling Frequency Fs	PLL2 Divide M	PLL2 Multiply N	Phase Comparison Frequency Fref [KHz]
64Fs	0.512	98.304	8 KHz	2	384	256
	1.024		16 KHz	4		
	2.048		32 KHz	8		
	4.096		64 KHz	16		
	8.192		128 KHz	32		
	0.7056	135.4752	11.025 KHz	2	384	352.8
	1.4112		22.05 KHz	4		
	2.8224		44.1 KHz	8		
	5.6448		88.2 KHz	16		
	11.2896		176.4 KHZ	32		
	0.768	147.456	12 KHz	2	384	384
	1.536		24 KHZ	4		
	3.072		48 KHz	8		
	6.144		96 KHz	16		
	12.288		192 KHz	32		

37. VCO frequency = 768×Fs×n (n = 16, 8, 4, 2, and 1)

Table 29. LOOP FILTER FOR PLL2

Loop filter	XT1 or BCLK	VCO [MHz]	Fref [KHz]	S3 (Note 38)	S2 (Note 38)	S1 (Note 38)	S0 (Note 38)	R1[kΩ] (Note 38)	R2[kΩ] (Note 38)	C1[pF] (Note 38)	C2[pF] (Note 38)
								typ	typ	typ	typ
Internal	XT1 = 12 MHz	98.304	96	0	1	1	0	–	–	–	–
		135.4752	19.2	1	0	0	1				
		147.456	96	0	1	1	0				
	XT1 = 19.2 MHz	98.304	768	0	0	1	0				
		135.4752	153.6	0	1	1	0				
		147.456	768	0	0	1	0				
	XT1 = 24 MHz	98.304	192	0	1	0	1				
		135.4752	38.4	1	0	0	0				
		147.456	192	0	1	0	1				
	BCLK = 32Fs	98.304	256	0	0	1	1				
		135.4752	352.8	0	0	1	1				
		147.456	384	0	0	1	1				
	BCLK = 48Fs	98.304	384	0	0	1	1				
		135.4752	264.6	0	0	1	1				
		147.456	288	0	0	1	1				
	BCLK = 64Fs	98.304	256	0	0	1	1				
		135.4752	352.8	0	0	1	1				
		147.456	384	0	0	1	1				
External	XT1 = 12 MHz	98.304	96	–				–	17.4 (Note 39)	348 (Note 39)	19100 (Note 39)
		135.4752	19.2								
		147.456	96								
	XT1 = 19.2 MHz	98.304	768						5.97 (Note 39)	370 (Note 39)	20300 (Note 39)
		135.4752	153.6								
		147.456	768								
	XT1 = 24 MHz	98.304	192						12.3 (Note 39)	348 (Note 39)	19300 (Note 39)
		135.4752	38.4								
		147.456	192								

38. Regarding internal loop filter use, appropriate loop filter parameters must be selected according to this table. Regarding external loop filter use, the loop filter parameters need to be attached externally.
39. Each value need to be supplied by external resistor and capacitor. Refer to PLL2 (Audio) in Application.
External loop filter depends on XT1 frequency regardless of whether BCLK = 32 Fs, 48Fs, or 64 Fs is used in PLL2.

Class−D AMP

Table 30. CLASS−D AMP

(AvddDAMPL = AVddDAMPR = 1.5 V, T_A = 25°C)

Item	Symbol	condition	Min	Typ	Max	Unit
On resistance	Ron	on resistance is set to minimum by register (Note 40)		0.61	2.57	Ω

40. Set 0x3ff00 to Drivability set register DZINP in “DAMPCTL” described in the “Audio Functions User’s Manual”.

XTAL Characteristics

Table 31. XTAL CHARACTERISTICS

(Vdd1(Note 41) = 0.95 to 1.155 V, VddXT1 = 0.95 to 1.155 V, T_A = −20°C to +65°C)

Item	Symbol	Min	Typ	Max	Unit
Frequency	Fmax	12		24	MHz

41. Power up and power down timing of VddXT1 and Vdd1 should be as close as possible. Note that the oscillation frequency of XT1 that can be used with this product depends on the following table.

Table 32. XT1 FREQUENCY

Function to be Used	Available Frequency of XT1 (✓ Means Available)			
	12 MHz	19.2 MHz	24 MHz	Other than the left
All functions	✓	✓	✓	(Note 42)

42. The frequencies of XT1 other than 12MHz, 19.2MHz, and 24MHz are not available, because some clock frequencies for PLL are determined internally based on the XTALINFO[1:0] terminal input during ROM boot.

XTALINFO[1:0] terminal input may be set to a frequency of 12 MHz, 19.2 MHz, or 24 MHz.

12bit ADC Converter Characteristic

Table 33. 12BIT ADC CONVERTER CHARACTERISTIC

(Vdd1 = 0.95 to 1.155 V, AVddADC = 1.70 to 1.95 V, T_A = −20°C to +65°C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin applied
ADC power supply voltage	AVDH		1.70		1.95	V	AVddADC
ADC GND voltage	AVDL		0			V	AVssADC
Analog input voltage	SIN		AVDL		AVDH	V	SIN[7: 0]
ADC resolution	BIT				12	Bit	SIN[7: 0]
ADC operating clock frequency (Note 43)	Fclk	fSPEED = 0 (Note 44)			16	MHz	
		fSPEED = 1 (Note 44)			3.2	MHz	
ADC conversion time	Tc		22			Cycle	
ADC sample rate	Fs	fSPEED = 0 (Note 44)			727	KS/s	
		fSPEED = 1 (Note 44)			145	KS/s	
Differential Linearity Error (Note 43)	DNL		−2		2	LSB	SIN[7: 0]
Linearity Error (Note 43)	INL		−3		3	LSB	SIN[7: 0]

43. Electrical specifications are based on simulation results.
44. Speed control bit in “ADC” described in the “System Functions User’s Manual ”.

USB2.0 PHY Characteristics

The USB−PHY supports the following standards.

- Universal Serial Bus Specification, Revision 2.0 (for Device only)
- Battery Charging Specification, Revision 1.2

AC CHARACTERISTICS

Reset

- [Condition]
  Vdd1 = 0.95 V to 1.155 V, Vdd2 = 1.7 V to 1.95 V or 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 15 pF to 40 pF

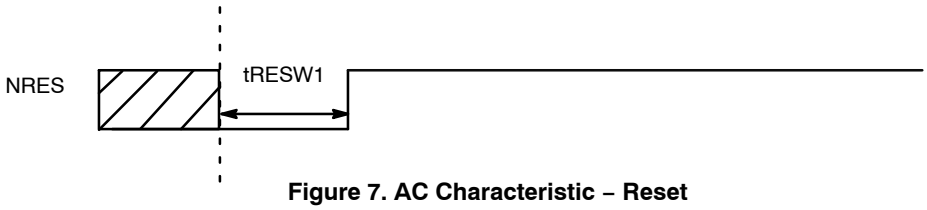


Figure 7. AC Characteristic − Reset

Table 34.

Item	Symbol	Condition	Min	Typ	Max	Unit
Resetting active period	tRESW1	Time after Vdd* reaches to recommended operating voltage	400	−	−	μs

*Refer to the “INTC” chapter in the “System Functions User’s Manual” for more detail if using noise filter, etc.

External Interrupt

- [condition]
  Vdd1 = 0.95 V to 1.155 V, Vdd2, VddSD1 = 1.7 to 1.95 V or 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 15 pF to 40 pF

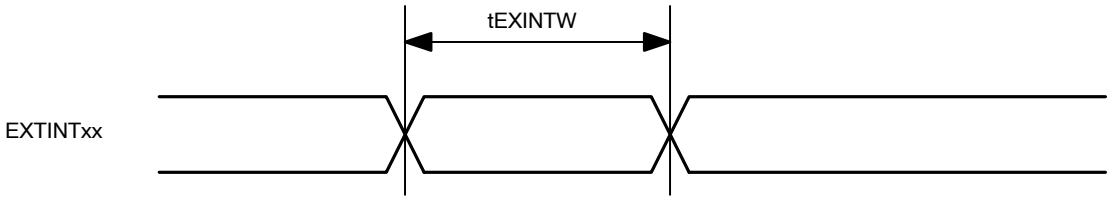


Figure 8. AC Characteristic − External Interrupt

Table 35.

Item	Symbol	Condition	Min	Typ	Max	Unit
Pulse width of external interrupt	tEXINTW	Set of interruption factor not use noise filter function	2	−	−	T

45. T: BASICCLK clock rate (frequency = Farm).

I2C

- [Condition]
  Vdd1 = 0.95 V to 1.155 V, Vdd2 = 1.7 V to 1.95 V or 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 15 pF to 40 pF

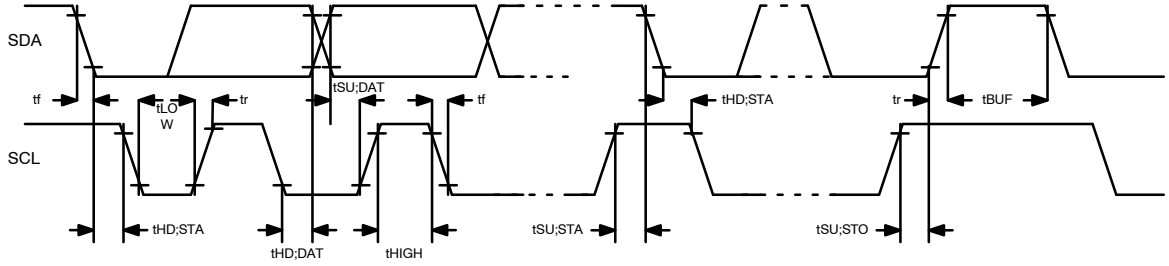


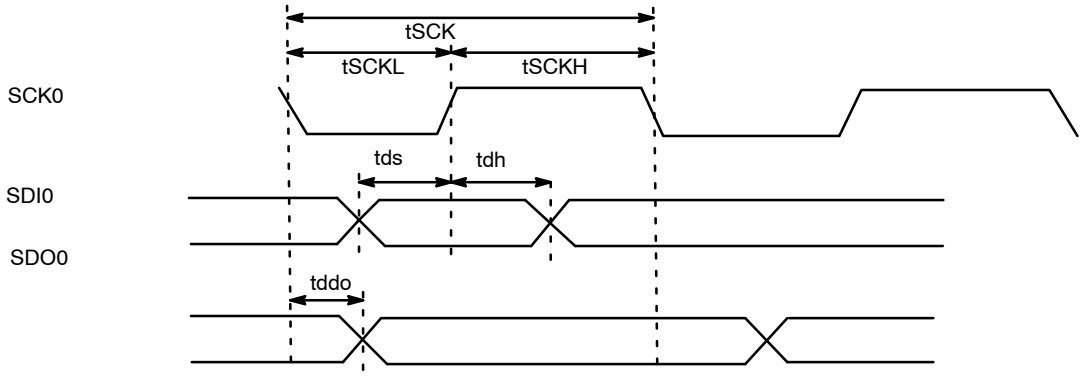
Figure 9. AC Characteristic − I2C

Table 36.

Item	Symbol	Standard mode		Full mode		Unit
		Min	Max	Min	Max	
SCL frequency	fSCL	0	100	0	400	kHz
Hold time START (repetition) condition (After this period, the first clock pulse is generated.)	tHD;STA	4.0	–	0.6	–	μs
Low period of SCL	tLOW	4.7	–	1.3	–	μs
High period of SCL	tHIGH	4.0	–	0.6	–	μs
Setup time of repetition START condition	tSU;STA	4.7	–	0.6	–	μs
Data hold time: (for master in accordance with CBUS)	tHD;DAT	5.0	3.45	0	0.9	μs
Data setup time	tSU;DAT	250	–	100	–	ns
Rise time SDA and SCL	Tr	–	1000	–	300	ns
Fall time SDA and SCL	Tf	–	300	–	300	ns
Setup time of STOP condition	tSU;STO	4.0	–	0.6	–	μs
Time of bus release between STOP and START condition	tBUF	4.7	–	1.3	–	μs

SPI Interface

- [Condition]
  Vdd1 = 0.95 V to 1.155 V, Vdd2 = 1.7 V to 1.95 V or 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 15 pF to 40 pF



46. When the polarity of SCK is changed, SCK in this Figure is inverted.

Figure 10. AC Characteristic − SPI Interface

Table 37.

Item	Symbol	min	typ	max	unit
SCLK rate	tSCK	8		−	T
SCLK LOW time	tSCKL	4		−	T
SCLK HIGH time	tSCKH	4		−	T
data setup time	tds	2		−	T
data hold time	tdh	2		−	T
data delay time	tddo	−		2	T

47. T: APB CLK rate (frequency = Fapb).

Serial Flash Interface

- [Condition]
  Vdd1 = 0.95 V to 1.155 V, Vdd2 = 1.7 V to 1.95 V or 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 6 to 30 pF

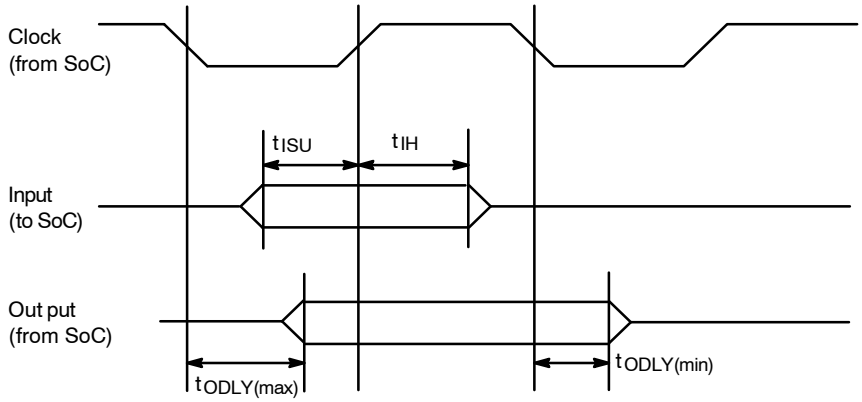


Figure 11. AC Characteristic − Serial Flash Interface

- [Applied Pin]
  - Clock: SCK1
  - Output: SDI1, SDO1, SWP1, SHOLD1, QSCS
  - Input: SDI1, SDO1, SWP1, SHOLD1

Table 38.

I/O Voltage (Vdd2)		2.7 V to 3.6 V		1.7 V to 1.95 V		
External Load / I/O Drivability		12 pF to 26 pF / 10 mA 6 pF to 12 pF / 8 mA		23 pF to 30 pF / 8 mA 10 pF to 23 pF / 4 mA		
Item	Symbol	Min	Max	Min	Max	Unit
SFIFSEL2 = 0 (Note 48)						
Input setup time	t_{ISU}	4.5	–	4.5	–	ns
Input hold time	t_{IH}	6.0	–	6.0	–	ns
Output Delay time	t_{ODLY}	1.0	5.5	1.0	5.5	ns
SFIFSEL2 = 1 (Note 48)						
Input setup time	t_{ISU}	4.8	–	4.8	–	ns
Input hold time	t_{IH}	7.0	–	7.0	–	ns
Output Delay time	t_{ODLY}	1.0	6.8	1.0	6.8	ns

48. SFIFSEL2 is the value of S−Flash I/F select register (SFIFSEL) bit2 described in “System Controller” described in the “System Functions User’s Manual”.

XMC External Memory Bus Timing

- [Condition]
  Vdd1 = 0.95 V to 1.155 V, Vdd2 = 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 15 pF to 40 pF

External Memory Bus Read

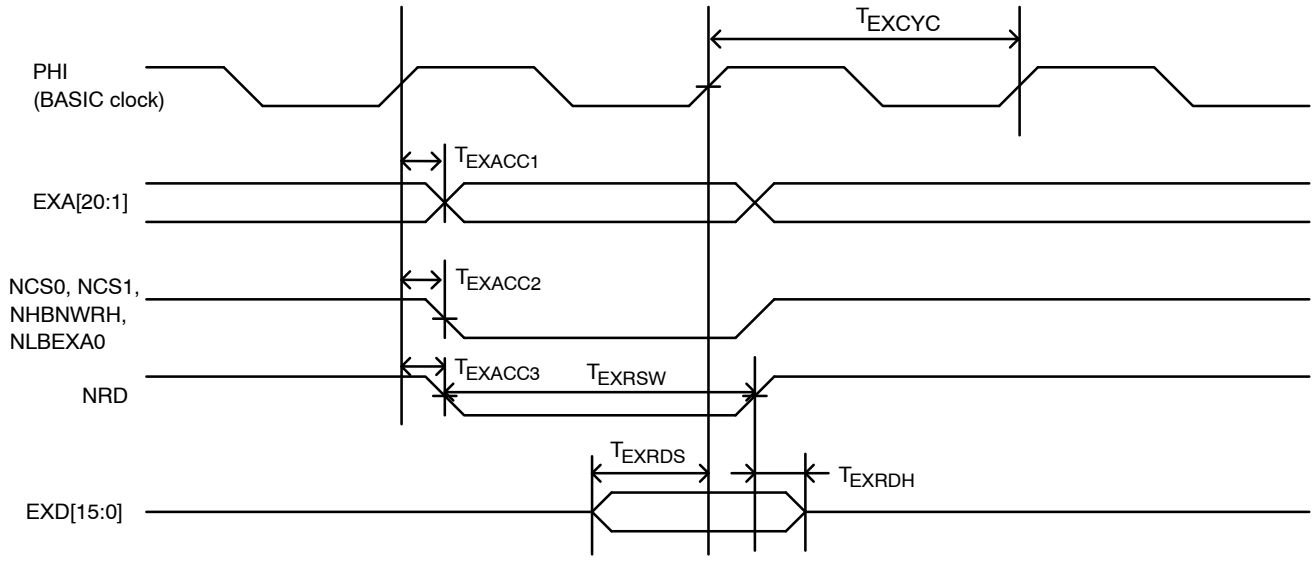


Figure 12. AC Characteristics − External Memory Bus Read Timing

External Memory Bus Write

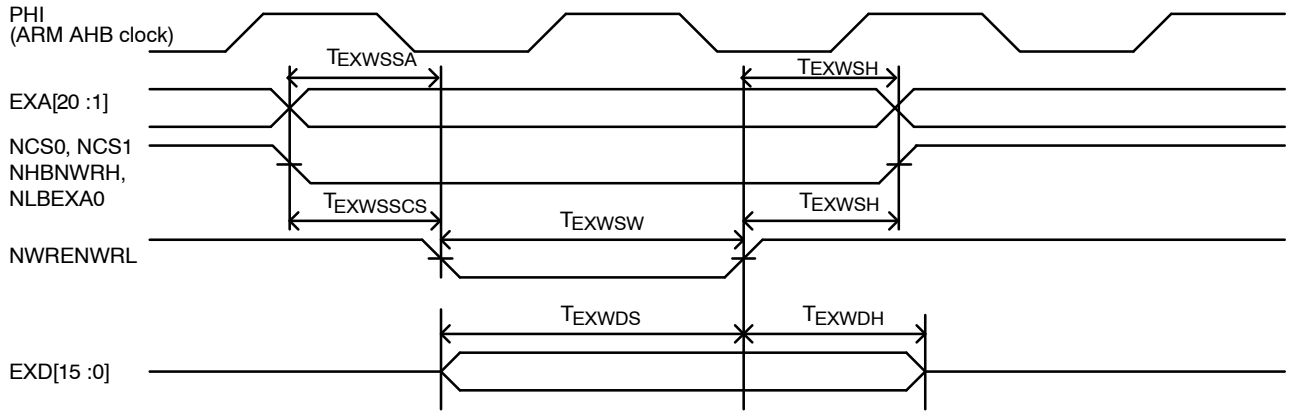


Figure 13. AC Characteristics – External Memory Bus Write Timing

Table 39.

Item	Symbol	Min	Typ	Max	Unit
CPU clock cycle time	T_{EXCYC}	–	1T	–	ns
Read data access time	T_{EXACC1}	–	–	13	ns
	T_{EXACC2}	–	–	Tacs + 13	ns
	T_{EXACC3}	–	–	Tacs + Tcos + 12	ns
Read data setup time	T_{EXRDS}	20	–	–	ns
Read data hold time	T_{EXRDH}	0	–	–	ns
Read strobe pulse width	T_{EXRSW}	Tpgwt + 1 T_{sub} – 12	–	–	ns
Write strobe pulse width	T_{EXWSW}	Tpgwt +1 T_{sub} – 5	–	–	ns
Write address setup time	T_{EXWSSA}	Tacs + Tcos + 0.5 T_{sub} – 10	–	–	ns
Write strobe setup time	$T_{EXWSSCS}$	Tcos + 0.5 T_{sub} – 5	–	–	ns
Write strobe hold time	T_{EXWSH}	Tcoh + 0.5 T_{sub} – 5	–	–	ns
Write data setup time	T_{EXWDS}	Tcos + Tpgwt + 1 T_{sub} – 10	–	–	ns
Write data hold time	T_{EXWDH}	Tcoh + 0.5 T_{sub} – 10	–	Tcoh + 0.5 T_{sub}	ns

49. T: BASIC clock rate (frequency = Farm).
Regarding Tacs, Tcos, Tpgwt, Tcoh, refer to the “XMC” chapter in the “System Functions User’s Manual”.
Even when Tpgwt (programmable wait register) = 1, equivalent to Tpgwt = 0.

SDRAM Interface

- [Condition]
  Vdd1 = 0.95 V to 1.155 V, Vdd2 = 1.7 V to 1.95 V or 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 5 to 15 pF

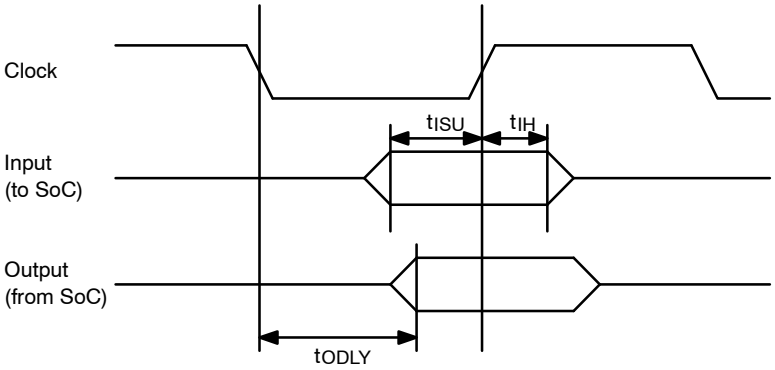


Figure 14. AC Characteristics − SDRAM Interface

- [Applied Pin]
  - Clock: SDRCLK
  - Output: SDRCKE, SDRCS, SDRWE, SDRCAS, SDRRAS, SDRDQM[1:0], SDRADDR[10:0], SDRBA[1:0], SDRDATA[15:0]
  - Input: SDRDATA[15:0]

Table 40.

I/O Voltage (Vdd2)		2.7 V to 3.6 V		1.7 V to 1.95 V		
External Load		5 pF to 15 pF				
I/O Drivability		8 mA		8 mA		
Item	Symbol	Min	Max	Min	Max	Unit
Input set−up time	t_{ISU}	2.8	–	2.8	–	ns
Input hold−up time	t_{IH}	1.8	–	1.8	–	ns
Output Delay time	t_{ODLY}	1.6	3.4	1.6	3.4	ns

50. Address becomes valid 1 cycle before the timing when CS becomes active. Address is stable while CS is active.

PSRAM Interface

- [Condition]
  Vdd1 = 0.95 V to 1.155 V, Vdd2 = 1.7 V to 1.95 V or 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 6 to 30 pF

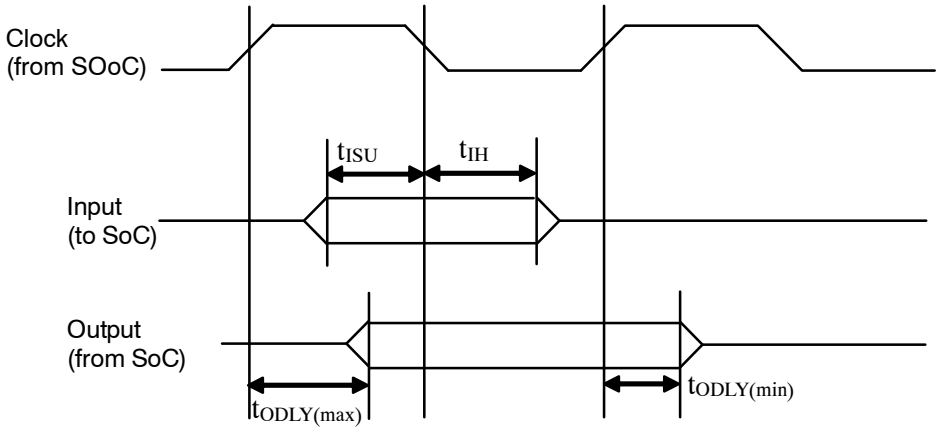


Figure 15. AC Characteristics − PSRAM Interface

- [Applied Pin]
  - Clock: PSM_SCK
  - Output: PSM_SDI, PSM_SDO, PSM_DAT2, PSM_DAT3, PSM_CS
  - Input: PSM_SDI, PSM_SDO, PSM_DAT2, PSM_DAT3

Table 41.

I/O voltage (Vdd2)		2.7V to 3.6V		1.7V to 1.95V		
External load / I/O drivability		12pF to 26pF / 10mA 6pF to 12pF / 8mA		23pF to 30pF / 8mA 10pF to 23pF / 4mA		
Item	Symbol	Min	Max	Min	Max	Unit
Input setup time	t_{ISU}	4.12	−	3	−	ns
Input hold time	t_{IH}	1.5	−	1.5	−	ns
Output Delay time	t_{ODLY}	2	7	2	7	ns

PCM Timing

- [Condition]
  Vdd1 = 0.95 V to 1.155 V, Vdd2 = 1.7 V to 1.95 V or 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 5 pF to 15 pF

Master Mode

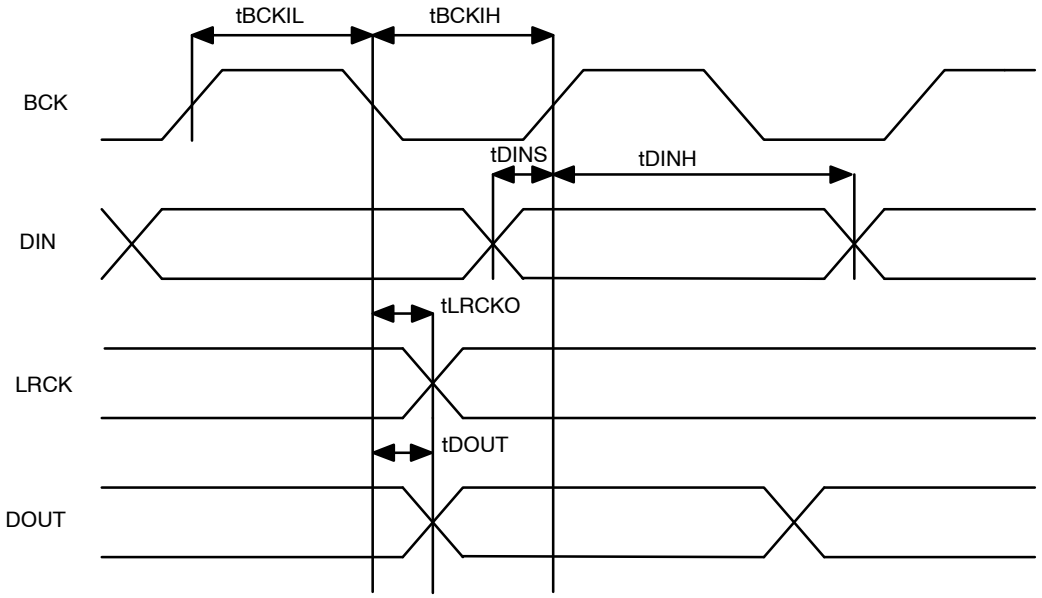


Figure 16. Master Mode

- [Applied Pin]
  - Clock: BCK0, BCK1
  - Output: LRCK0, LRCK1, DOUT0, DOUT1
  - Input: DIN0, DIN1

Table 42.

I/O Voltage (Vdd2)		2.7 V to 3.6 V		1.7 V to 1.95 V		
External Load / I/O Drivability		8 pF to 15 pF / 8 mA 5 pF to 8 pF / 4 mA		8 pF to 15 pF / 8 mA 5 pF to 8 pF / 4 mA		
Item	Symbol	Min	Max	Min	Mix	Unit
BCKI Low period	tBCKIL	38.0	–	38.0	–	ns
BCKI High period	tBCKIH	38.0	–	38.0	–	ns
DIN setup time	tDINS	8.0	–	8.0	–	ns
DIN hold time	tDINH	9.0	–	8.0	–	ns
LRCK delay time	tLRCKO	−13.0	13.0	−11.5	11.5	ns
DOUT delay time	tDOUT	−13.0	13.0	−11.5	11.5	ns

Slave Mode

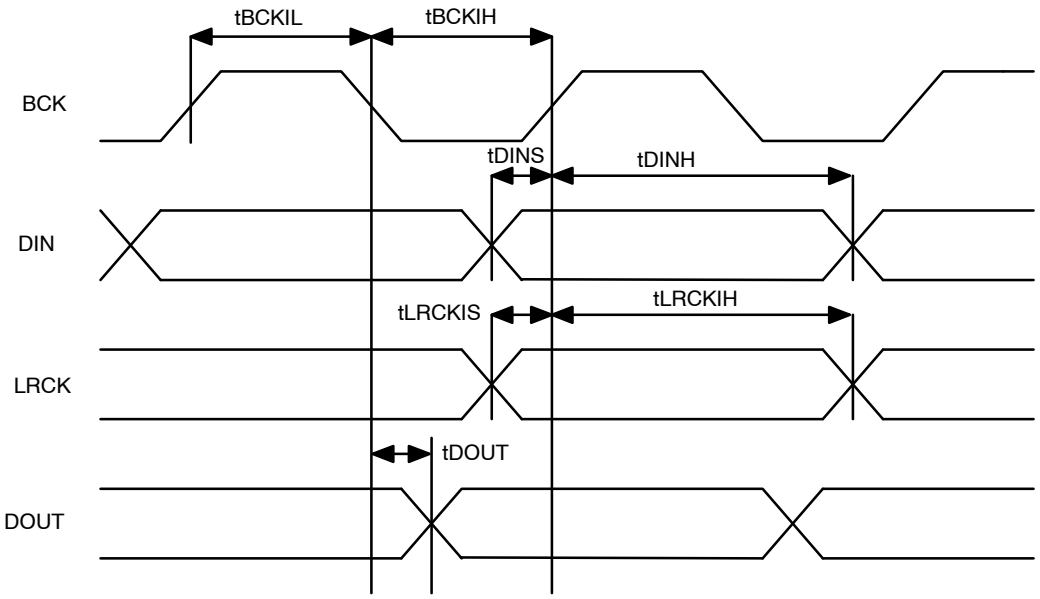


Figure 17. Slave Mode

- [Applied Pin]
  - Clock: BCK0, BCK1
  - Output: DOUT0, DOUT1
  - Input: LRCK0, LRCK1, DIN0, DIN1

Table 43.

I/O Voltage (Vdd2)		2.7 V to 3.6 V		1.7 V to 1.95 V		
External Load / I/O Drivability		8 pF to 15 pF / 8 Ma 5 pF to 8 pF / 4 mA		8 pF to 15 pF / 8 mA 5 pF to 8 pF / 4 mA		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
BCKI Low period	tBCKIL	30.0	–	30.0	–	ns
BCKI High period	tBCKIH	30.0	–	30.0	–	ns
DIN setup time	tDINS	8.0	–	8.0	–	ns
DIN hold time	tDINH	8.0	–	8.0	–	ns
LRCK setup time	tLRCKIS	8.0	–	8.0	–	ns
LRCK hold time	tLRCKIH	8.0	–	8.0	–	ns
DOUT delay time	tDOUT	−13.0	13.0	−11.5	11.5	ns

SD Card Interface Timing

- [Condition]
  Vdd1 = 0.95 V to 1.155 V, VddSD0, VddSD1 = 1.7 V to 1.95 V or 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 6 to 40 pF

Normal (Default) Mode

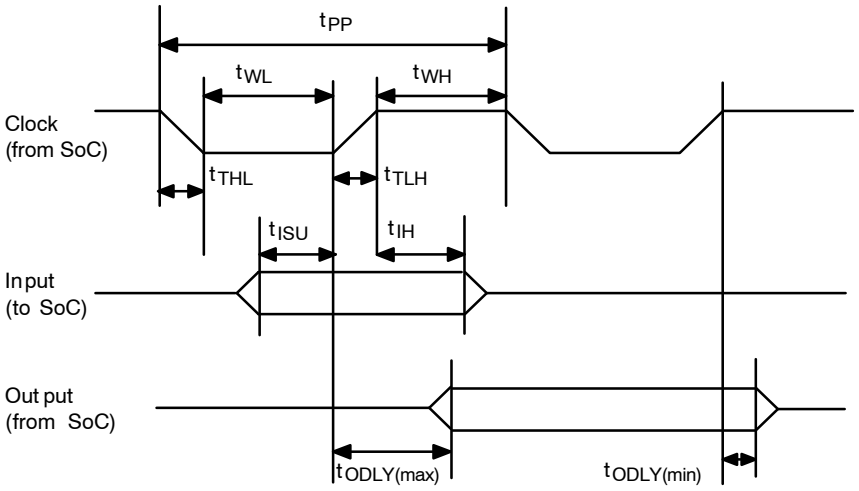


Figure 18. Normal (Default) Mode

- [Applied Pin]
  - Clock: SDCLK0, SDCLK1, SDCLK2
  - Output: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]
  - Input: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]

Table 44.

I/O Voltage (VddSD0, VddSD1)		2.7 V to 3.6 V		
External Load / I/O Drivability		12 pF to 40 pF / 10 Ma 6 pF to 12 pF / 8 mA		
Item	Symbol	Min	Max	Unit
Clock Frequency	f_{PP}	0	25	MHz
Clock low time	t_{WL}	10	–	ns
Clock high time	t_{WH}	10	–	ns
Clock rise time	t_{TLH}	–	10	ns
Clock fall time	t_{THL}	–	10	ns
Input set−up time (from SD to SoC)	t_{ISU}	5.9	–	ns
Input hold−up time (from SD to SoC)	t_{IH}	0	–	ns
Output Delay time during Data Transfer Mode (from SoC to SD)	t_{ODLY}	5.1	14.0	ns

High−Speed Mode

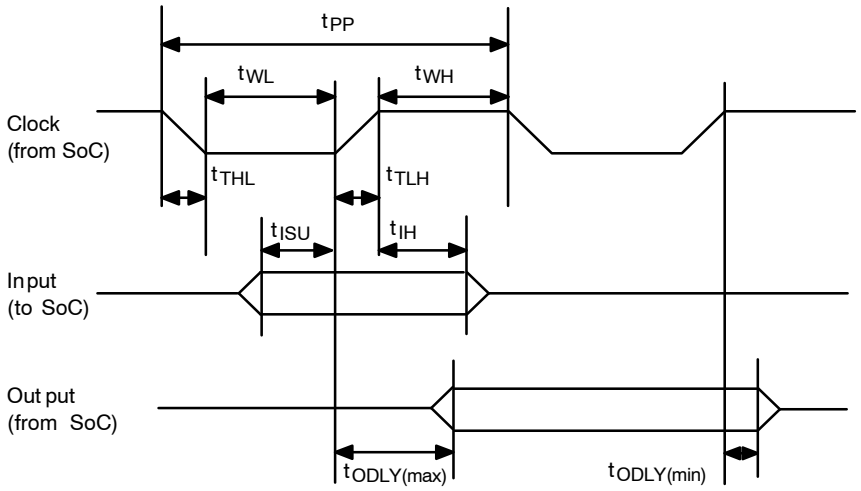


Figure 19. High−Speed Mode

- [Applied Pin]
  - Clock: SDCLK0, SDCLK1, SDCLK2
  - Output: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]
  - Input: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]

Table 45.

I/O Voltage (VddSD0, VddSD1)		**2.7 V to 3.6 V**		
External Load / I/O Drivability		**12 pF to 40 pF / 10 mA 6 pF to 12 pF / 8 mA**		
Item	**Symbol**	**Min**	**Max**	**Unit**
Clock Frequency	f_{PP}	0	50	MHz
Clock low time	t_{WL}	7	–	ns
Clock high time	t_{WH}	7	–	ns
Clock rise time	t_{TLH}	–	3	ns
Clock fall time	t_{THL}	–	3	ns
Input set−up time (from SD to SoC)	t_{ISU}	5.9	–	ns
Input hold−up time (from SD to SoC)	t_{IH}	2.5	–	ns
Output Delay time (from SoC to SD)	t_{ODLY}	14.0	2.0	ns

SDR25 Mode

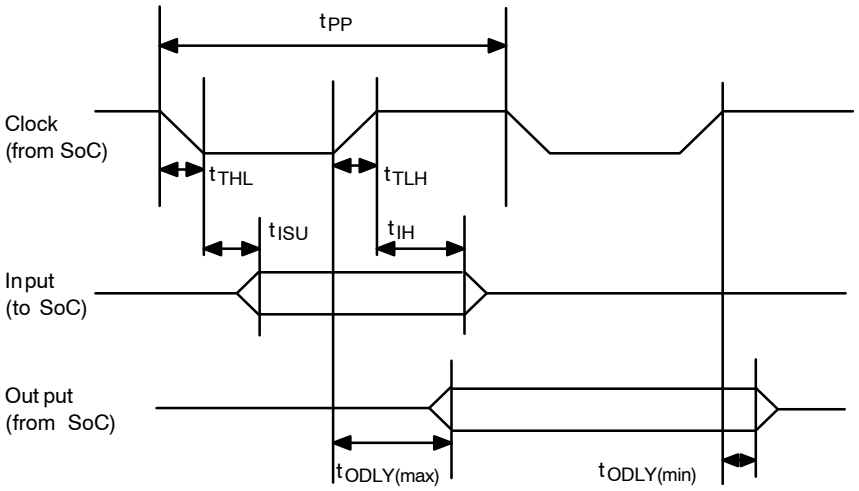


Figure 20. SDR25 Mode

- [Applied Pin]
  - Clock: SDCLK0, SDCLK1, SDCLK2
  - Output: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]
  - Input: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]

Table 46.

I/O Voltage (VddSD0, VddSD1)		**1.7 V to 1.95 V**		
External Load / I/O Drivability		**23 pF to 30 pF / 8 mA 15 pF to 23 pF / 4 mA 10 pF to 15 pF / 2 mA**		
Item	**Symbol**	**Min**	**Max**	**Unit**
Clock Frequency	f_{PP}	0	50	MHz
Clock rise time	t_{TLH}	–	2.9	ns
Clock fall time	t_{THL}	–	2.9	ns
Input set−up time (from SD to SoC)	t_{ISU}	5.9	–	ns
Input hold−up time (from SD to SoC)	t_{IH}	1.5	–	ns
Output Delay time (from SoC to SD)	t_{ODLY}	0.9	17.0	ns

SDR50 Mode

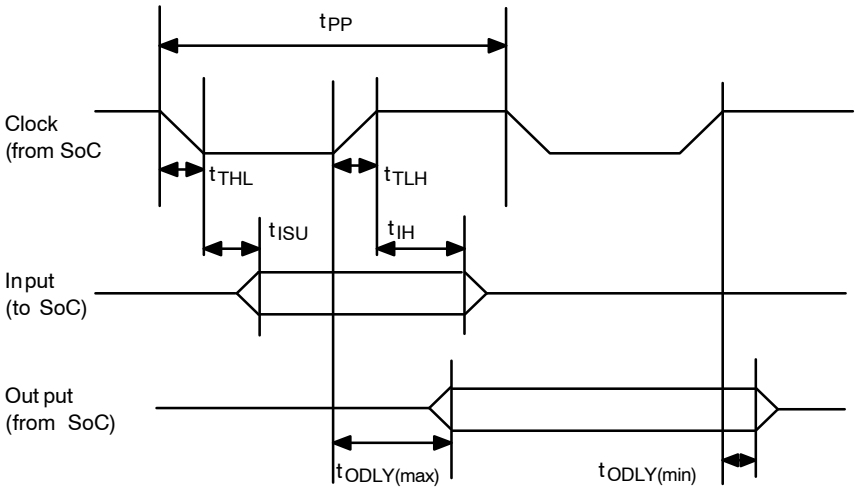


Figure 21. SDR50 Mode

- [Applied Pin]
  - Clock: SDCLK0, SDCLK1, SDCLK2
  - Output: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]
  - Input: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]

Table 47.

I/O Voltage (VddSD0, VddSD1)		**1.7 V to 1.95 V**		
External Load / I/O Drivability		**23 pF to 30 pF / 8 mA 15 pF to 23 pF / 4 mA 10 pF to 15 pF / 2 mA**		
Item	**Symbol**	**Min**	**Max**	**Unit**
Clock Frequency	f_{PP}	0	57	MHz
Clock rise time	t_{TLH}	–	2.9	ns
Clock fall time	t_{THL}	–	2.9	ns
Input set−up time (from SD to SoC)	t_{ISU}	8.0	–	ns
Input hold−up time (from SD to SoC)	t_{IH}	1.4	–	ns
Output Delay time (from SoC to SD)	t_{ODLY}	0.9	14.6	ns

DDR50 Mode

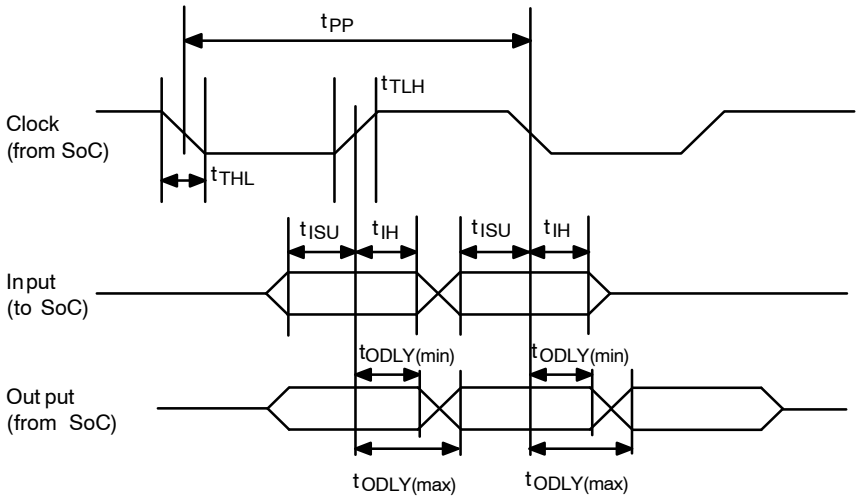


Figure 22. DDR50 Mode

- [Applied Pin]
  - Clock: SDCLK0, SDCLK1, SDCLK2
  - Output: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]
  - Input: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]

Table 48.

I/O Voltage (VddSD0, VddSD1)		**1.7 V to 1.95 V**		
External Load / I/O Drivability		**23 pF to 30 pF / 8 mA 15 pF to 23 pF / 4 mA 10 pF to 15 pF / 2 mA**		
Item	**Symbol**	**Min**	**Max**	**Unit**
Clock Frequency	f_{PP}	0	40	MHz
Clock rise time	t_{TLH}	–	2.9	ns
Clock fall time	t_{THL}	–	2.9	ns
Input set−up time (from SD to SoC)	t_{ISU}	5.0	–	ns
Input hold−up time (from SD to SoC)	t_{IH}	1.4	–	ns
Output Delay time (from SoCI to SD)	t_{ODLY}	0.9	9.5	ns

eMMC Interface Timing

- [Condition]
  Vdd1 = 0.95 V to 1.155 V, VddSD0, VddSD1 = 1.7 V to 1.95 V or 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 6 to 40 pF

Normal (Default) Mode

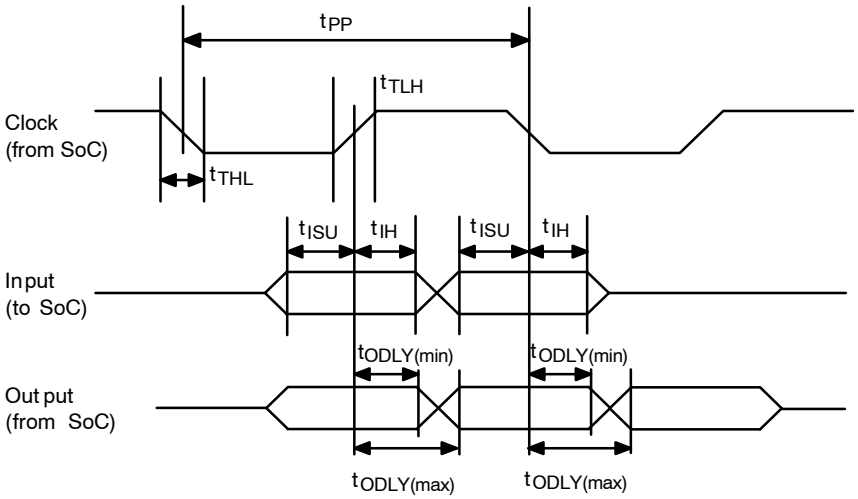


Figure 23. Normal (Default) Mode

- [Applied Pin]
  - Clock: SDCLK0, SDCLK1, SDCLK2
  - Output: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]
  - Input: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]

Table 49.

I/O Voltage (VddSD0, VddSD1)		**2.7 V to 3.6 V**		**1.7 V to 1.95 V**		
External Load / I/O Drivability		**12 pF to 40 pF / 10 mA 6 pF to 12 pF / 8 mA**		**23 pF to 30 pF / 8 mA 15 pF to 23 pF / 4 mA 10 pF to 15 pF / 2 mA**		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Clock Frequency	f_{PP}	0	26	0	26	MHz
Clock low time	t_{WL}	10	–	10	–	ns
Clock high time	t_{WH}	10	–	10	–	ns
Clock rise time	t_{TLH}	–	3	–	3	ns
Clock fall time	t_{THL}	–	3	–	3	ns
Input set−up time (from SD to SoC)	t_{ISU}	11.5	–	11.5	–	ns
Input hold−up time (from SD to SoC)	t_{IH}	9.0	–	9.0	–	ns
Output Delay time (from SoC to SD)	t_{ODLY}	10.0	27.5	10.0	27.5	ns

High−Speed SDR Mode

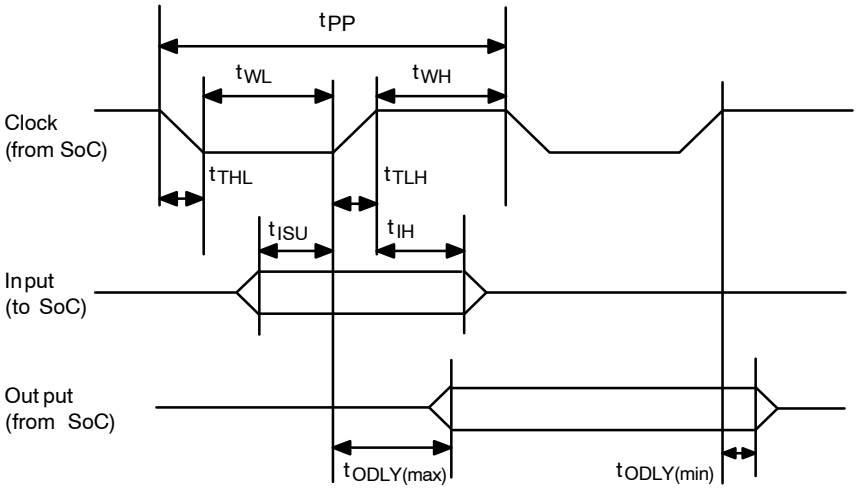


Figure 24. High−Speed SDR Mode

- [Applied Pin]
  - Clock: SDCLK0, SDCLK1, SDCLK2
  - Output: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]
  - Input: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]

Table 50.

I/O Voltage (VddSD0, VddSD1)		**2.7 V to 3.6 V**		**1.7 V to 1.95 V**		
External Load / I/O Drivability		**12 pF to 40 pF / 10 mA 6 pF to 12 pF / 8 mA**		**23 pF to 30 pF / 8 mA 15 pF to 23 pF / 4 mA 10 pF to 15 pF / 2 mA**		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Clock Frequency	f_{PP}	0	52	0	52	MHz
Clock low time	t_{WL}	7	–	7	–	ns
Clock high time	t_{WH}	7	–	7	–	ns
Clock rise time	t_{TLH}	–	3	–	3	ns
Clock fall time	t_{THL}	–	3	–	3	ns
Input set−up time (from SD to SoC)	t_{ISU}	5.4	–	5.4	–	ns
Input hold−up time (from SD to SoC)	t_{IH}	3.0	–	3.0	–	ns
Output Delay time (from SoC to SD)	t_{ODLY}	3.0	16.1	3.0	16.1	ns

High−Speed DDR Mode

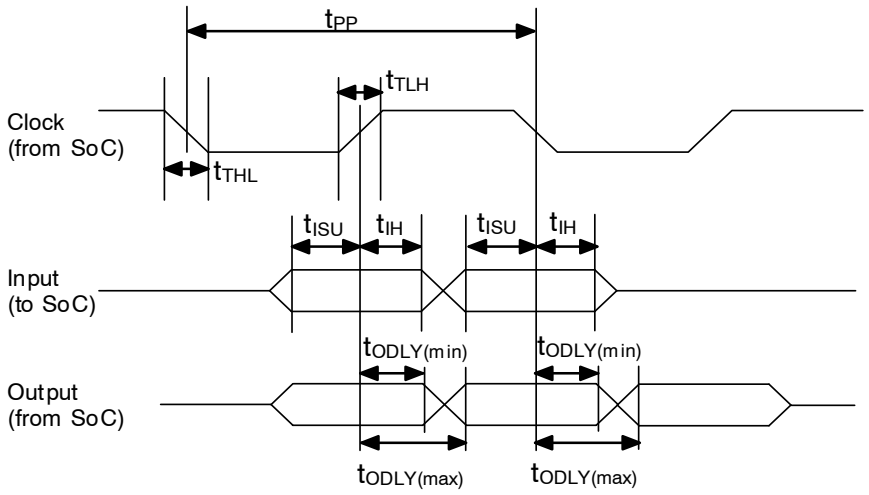


Figure 25. High−Speed DDR Mode

- [Applied Pin]
  - Clock: SDCLK0, SDCLK1, SDCLK2
  - Output: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]
  - Input: SDCMD0, SDCMD1, SDCMD2, SDAT0[3:0], SDAT1[3:0], SDAT2[3:0]

Table 51.

I/O Voltage (VddSD0, VddSD1)		2.7 V to 3.6 V		1.7 V to 1.95 V		
External Load / I/O Drivability		12 pF to 40 pF / 10 mA 6 pF to 12 pF / 8 mA		23 pF to 30 pF / 8 mA 15 pF to 23 pF / 4 mA 10 pF to 15 pF / 2 mA		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Clock Frequency	f_{PP}	0	30	0	33	MHz
Clock rise time	t_{TLH}	–	3	–	3	ns
Clock fall time	t_{THL}	–	3	–	3	ns
INPUT CMD						
Input set−up time (from SD to SoC)	t_{ISU}	19.5	–	16.4	–	ns
Input hold−up time (from SD to SoC)	t_{IH}	2.4	–	2.4	–	ns
OUTPUT CMD						
Output Delay time (from SoC to SD)	t_{ODLY}	3.0	29.0	3.0	26.0	ns
INPUT DAT						
Input set−up time (from SD to SoC)	t_{ISU}	9.6	–	8.1	–	ns
Input hold−up time (from SD to SoC)	t_{IH}	1.4	–	1.4	–	ns
OUTPUT DAT						
Output Delay time (from SoC to SD)	t_{ODLY}	2.5	14.1	2.5	12.6	ns

Digital Mic Timing

- [Condition]
  Vdd1 = 0.95 V to 1.155 V, Vdd2 = 1.7 V to 1.95 V or 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 15 pF to 40 pF

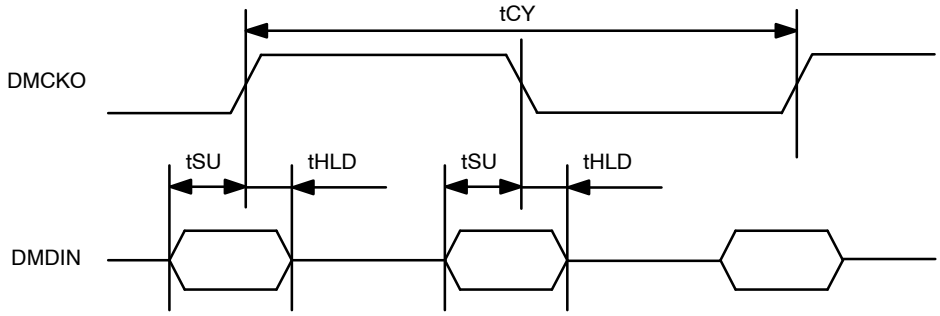


Figure 26. Digital Mic Timing

- [Applied Pin]
  - Clock: DMCKO0, DMCKO1
  - Input: DMDIN0, DMDIN1

Table 52.

Item	Symbol	Min	Typ	Max	Unit
Period of clock cycle (Note 51)	tCY	–		3.25	MHz
Clock duty		60:40		40:60	
Data setup time	tSU	40		–	ns
Data hold time	tHLD	0		–	ns

51. Internal clock and register setting.

UART Timing

- [Condition]
  Vdd1 = 0.95 V to 1.155 V, Vdd2= 1.7 V to 1.95 V or 2.7 V to 3.6 V, T_A = −20°C to +65°C
  External load 10 pF to 30 pF (Vdd2 = 1.7 V to 1.95 V), 10 pF to 40 pF (Vdd2 = 2.7 V to 3.6 V)

CTS Timing

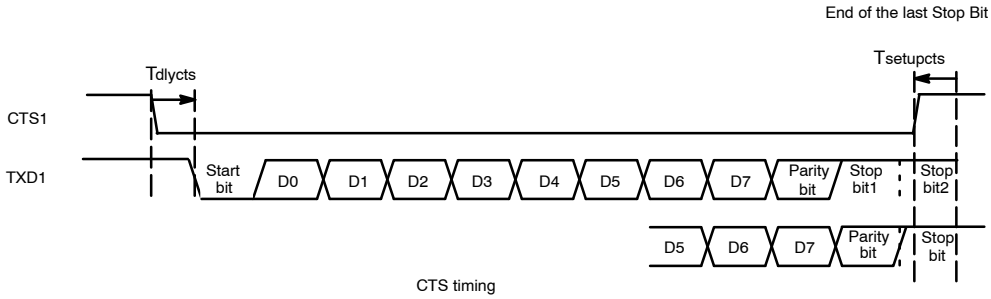


Figure 27. CTS Timing

- [Applied Pin]
  - Input: CTS1
  - Output: TXD1

Table 53.

Item	Condition	Symbol	Min	Max	Unit
Delay time	Completing preparation to transmit the current TXD data by setting registers at CTS1 = high From the negative edge	Tdlycts	–	6T+20	ns
CTS Setup time (not to transmit the next TXD data)	From end of the last StopBit	Tsetupcts	3T+20	–	ns

52. T: UART functional clock rate
53. In using hardware flow control by CTS/RTS, if the CTS setup time above is NOT met, the next TXD data will be transmitted at the time of having prepared it regardless of the CTS level.

RTS Timing

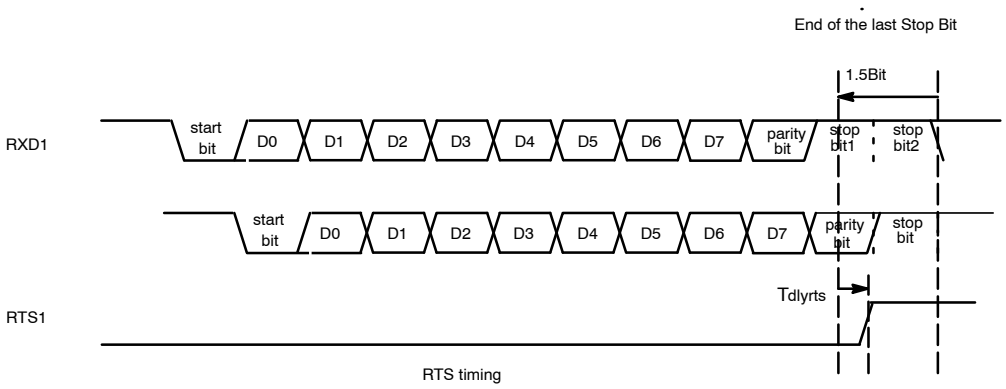


Figure 28. RTS Timing

- [Applied Pin]
  - Input: RXD1
  - Output: RTS1

Table 54.

Item	Condition	Symbol	Min	Max	Unit
Delay Time	Receiving the current RXD data with 15 bytes of data existing in the Reception FIFO or Receiving the current RXD data without using Reception FIFO From 1.5 bits before the end of the last StopBit	Tdlyrts	–	4T+20	ns

54. T: UART functional clock rate

APPLICATION

XTAL

For oscillation

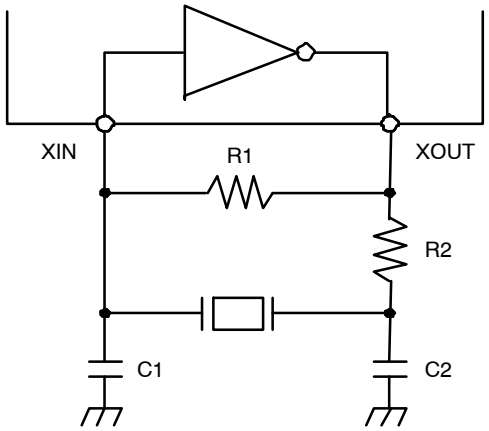


Figure 29. For Oscillation

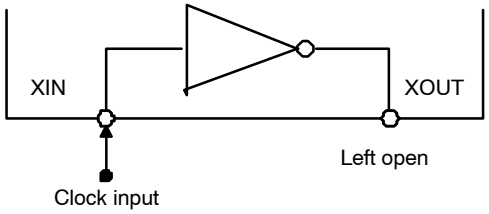
Table 55.

Symbol	XT1 XIN1/XOUT1	XTRTC XIN32K/XOUT32K
	24MHz	**32.768 KHz**
Example of crystal device	RIVER ELETEC FCX−07L	RIVER ELETEC TFX−03
R1	Open	10 MΩ
R2	0 Ω	0 Ω
C1	10pF	18pF
C2	10pF	18pF

55. Optimize the circuit constant for each product when you use this oscillation cell and ask to the manufacturer of the crystal device to investigate (matching investigation) because the best circuit constant changes depending on the specification of the crystal device used and the ambient surrounding (parasitic capacitance etc. of an external substrate).
56. The part values are for reference only. Adjustments may be required depending on the specific setup.
57. The following may be needed as the anti−noise measures of oscillation circuit.
    - Components should be as adjacent as possible, with shortened wiring between elements such as this SoC and the crystal device.
    - GND of the oscillation circuit should be as close as possible to GND (VSS) of this SoC.
    - Do not bring the wiring pattern of the large current drive close to the oscillation circuit.
    - Take wide pattern to avoid the effect of interference of other signals.

For input from external clock source (XT1)

Do as follows when using the external clock signal that is generated outside of the SoC by the oscillation module, etc. XT1 can be connected to an external clock signal that is generated outside of the SoC using the circuit shown in Figure 30. However, XTRTC cannot be connected to an external clock source.



NOTE: Input the signal of full amplitude to XIN (external clock input).

Figure 30. For Input from External Clock Source (XT1)

Table 56.

Item	Symbol	min	max	unit
H level input voltage (Note 58)	V_{IH}	VddXT1× 0.8	VddXT1 + 0.3	V
L level input voltage (Note 58)	V_{IL}	−0.3	VddXT1 × 0.25	V

58. There is no VIH/VIL specification at the input part of the xtal oscillator cell. The values are for reference when using external clock source.

- There is a possibility of influencing the signal quality when there is a long wire pattern on a circuit board of XOUT (The terminal opens). Therefore, recommend to cut the wire pattern on a circuit board or no wire pattern on it
- The xtal oscillator is supposed to be used with quartz resonator or ceramic resonator, we have no plan to evaluate this SoC in case of input from external clock source

PLL1(System)

The configuration of the PLL1 circuit is shown below.

Decoupling capacitors must be placed as close as possible to the power terminals (AVddPLL1 and AVssPLL1) of this SoC.

The power supply of PLL1 should be separated from other power supply lines to eliminate noise.

When using an Internal Loop Filter

VCNT1 must be open in this case.

When using an External Loop Filter

Refer to Table 25 for the recommended values of R2, C1, and C2.

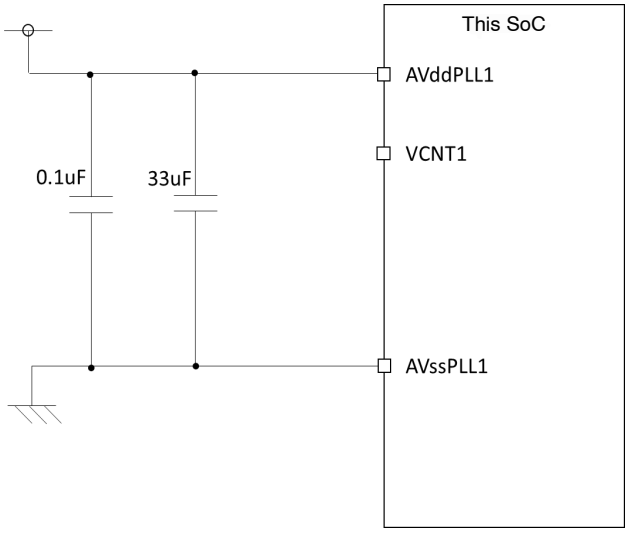


Figure 31. PLL1(System) for Internal Loop Filter

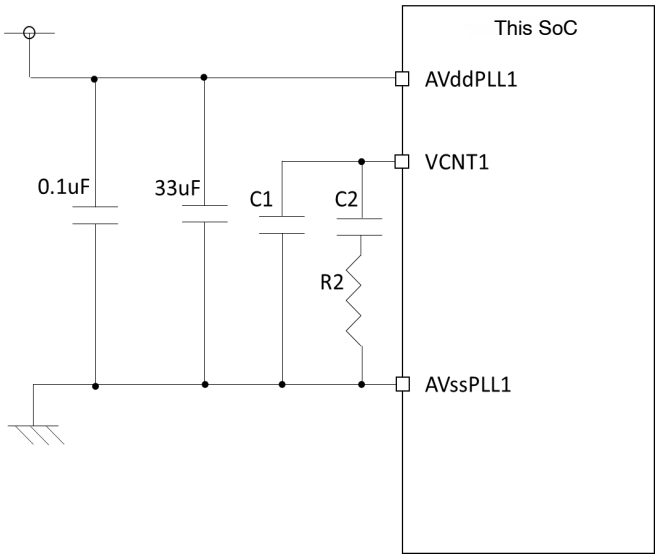


Figure 32. PLL1(System) for External Loop Filter

59. The part values are for reference only. Adjustments may be required depending on the specific setup.

PLL2(Audio)

The configuration of the PLL2 circuit is shown below.

Decoupling capacitors must be placed as close as possible to the power terminals (AVddPLL2 and AVssPLL2) of this SoC.

The power supply of PLL2 should be separated from other power supply lines to eliminate noise.

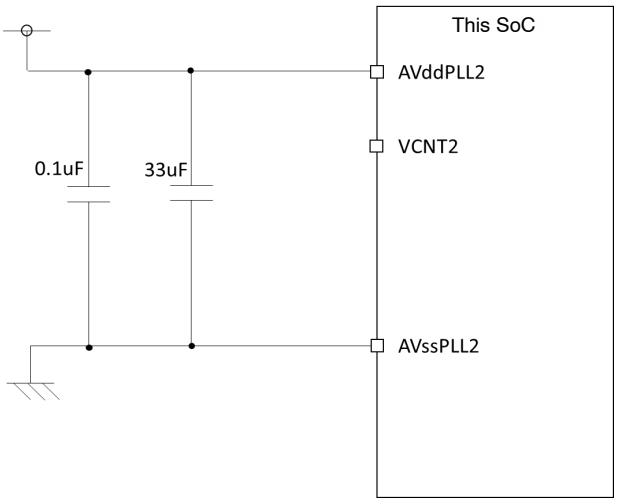


Figure 33. PLL2(Audio) for Internal Loop Filter

When using an Internal Loop Filter

VCNT2 must be open in this case.

When using an External Loop Filter

Refer to Table 29 for the recommended values of R2, C1, and C2.

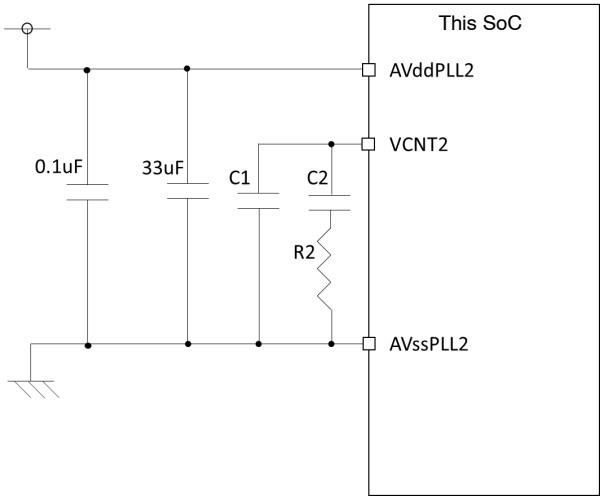


Figure 34. PLL2(Audio) for External Loop Filter

60. The part values are for reference only. Adjustments may be required depending on the specific setup.

12bit AD converter

The configuration of the ADC circuit is shown below.

Power supply decoupling should be done according to the figure below. At least the 0.1 μF capacitor should be ceramic (good quality), and must be placed as close as possible to this SoC.

You should supply clean Power and Ground to AVddADC and AVssADC.

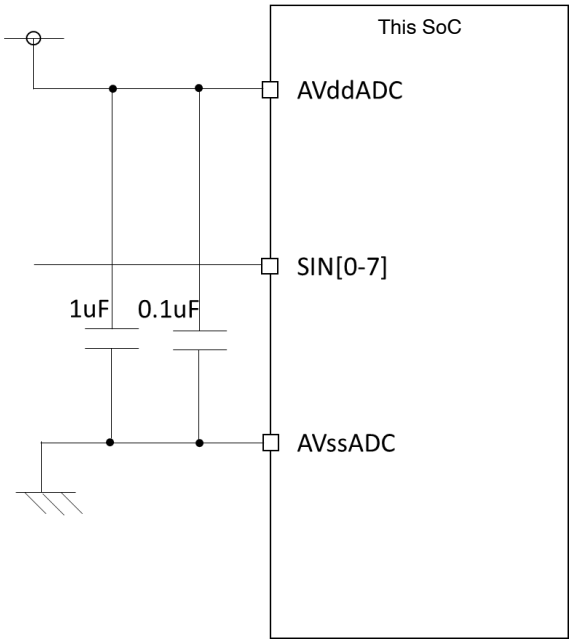


Figure 35. 12bit AD Converter

61. It is important that the wiring resistance is accurate in order to achieve the correct ADC conversion result. Also, pay attention to maintaining low noise.
62. Unused input pins of SIN[0−7] should be directly connected to AVssADC.

USB2.0 PHY

The configuration of the USB−PHY circuit for the Device is shown below.

USB Device

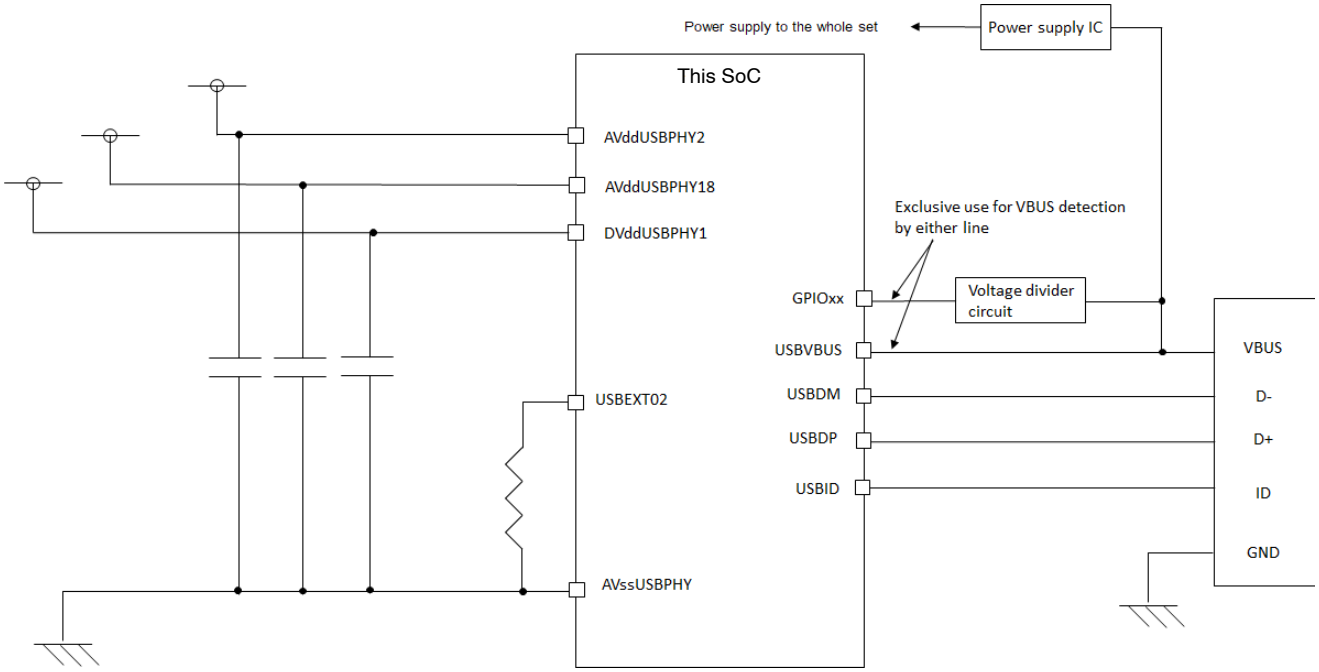


Figure 36. USB 2.0 PHY

Please refer to the “LC823455 USB2.0 Application Design Guideline” for details.

Class−D AMP

The configuration of the Class−D AMP circuit is shown below.

Single−End Form

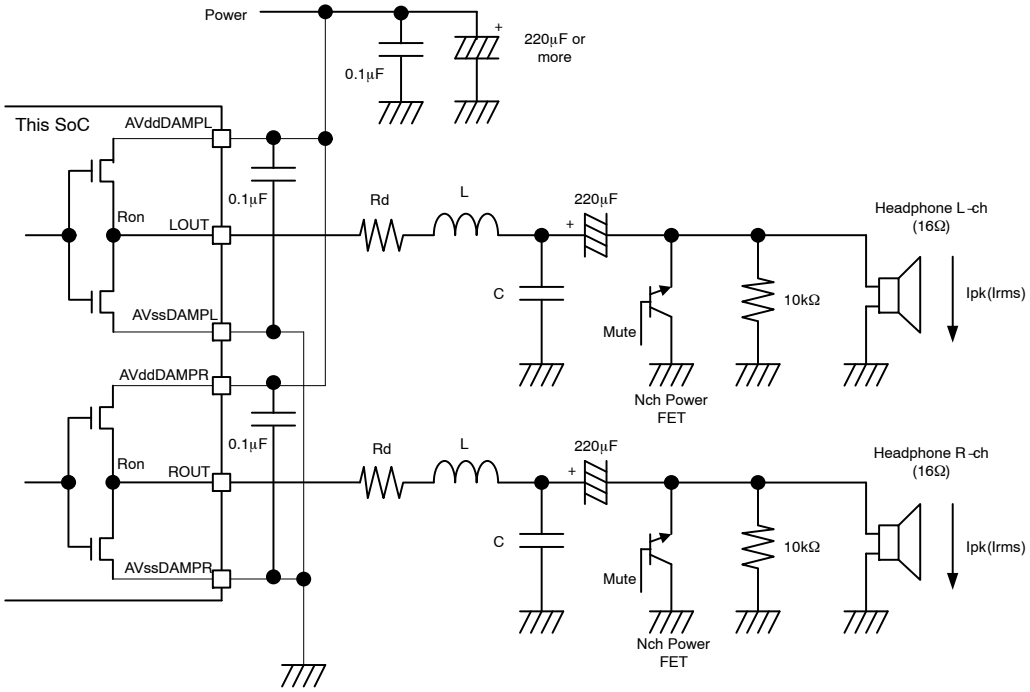


Figure 37. Class−D AMP in Single−End Form

BTL Form

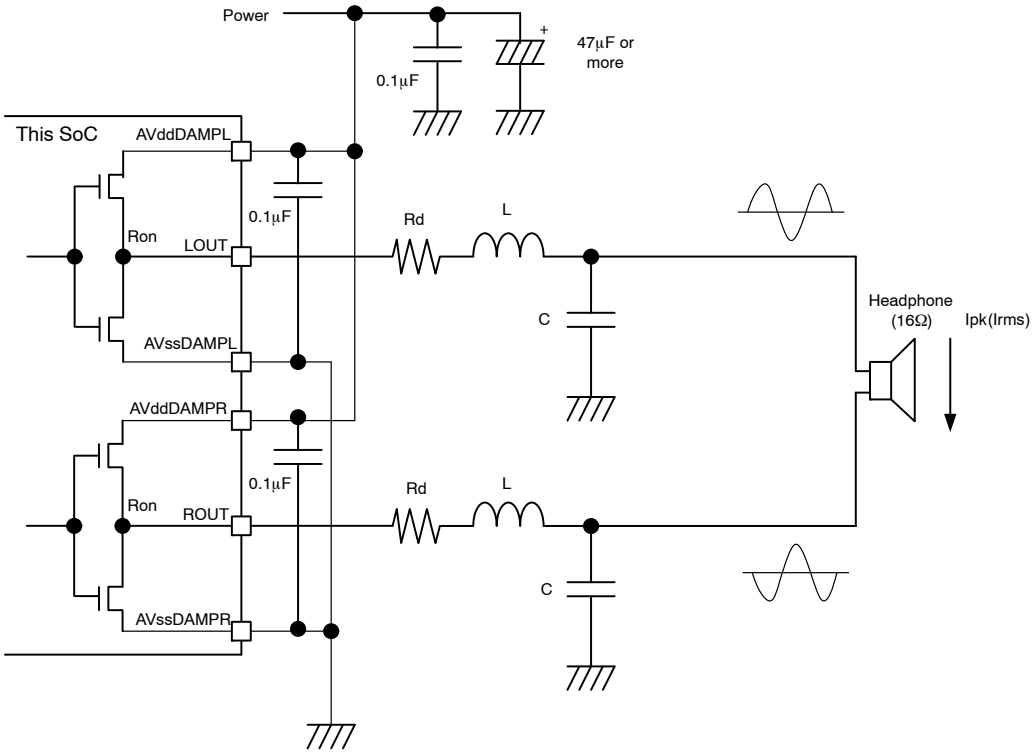


Figure 38. Class−D AMP in BTL Form

LCR Filter Example	L (μH)	C (μF)	Rd (Ω)
Type A	220	0.22	0 – 10
Type B	47	1	5 – 10

63. Rd doesn't include parasitic resistance of L.
64. Add a bypass condenser (0.1 μF) between AVddDAMPL and AVssDAMPL, AVddDAMPR and AVssDAMPR as close as possible to the terminals
65. Add a large electrolyte capacitor (220μF or more recommended) to AVddDAMPL, AVddDAMPR terminal for Single−End form to reject the noise and reduce the pumping phenomenon of Class−D AMP.
66. Check the voltage level of AVddDAMPL, AVddDAMPR and make sure not to exceed 1.65 V (recommended operating voltage) by using playback of 20 Hz, 0db (full scale) sine wave
67. Resistor Rd reduces the output level of Class−D AMP, and is related to the values of L and C used. Please choose a resistance value (Rd) to fit the actual system. Please note that Rd value must be determined based on the parasitic resistance of the inductor L.
68. While the Class−D AMP outputs LOUT and ROUT are used as GPO, the maximum supply voltage to AVddDAMPL and AVddDAMPR is 1.95 V. In this case, the LC filter cannot be connected to LOUT and ROUT to avoid damage from overvoltage via the pumping phenomenon.

Power Supply

Class−D AMP power supply to (AVddDAMPL, AVddDAMPR) must use a transient response and good power supply. When using a power supply where the transient response is bad and the capacity of the capacitor is small, a peculiar pumping phenomenon to the Class−D AMP is generated. The power supply voltage must not exceed the recommended operating range when the pumping phenomenon occurs.

The Class−D AMP output is PWM. The power supply noise affects the output of the Class−D AMP.

Power sources which have large internal impedance such as dry cell should not be directly connected to the power supply of the Class−D AMP, and those which have large switching noise such as switching regulator are not suitable and need to be taken care of.

Digital Mic

The configuration of the Digital Mic circuit is shown below.

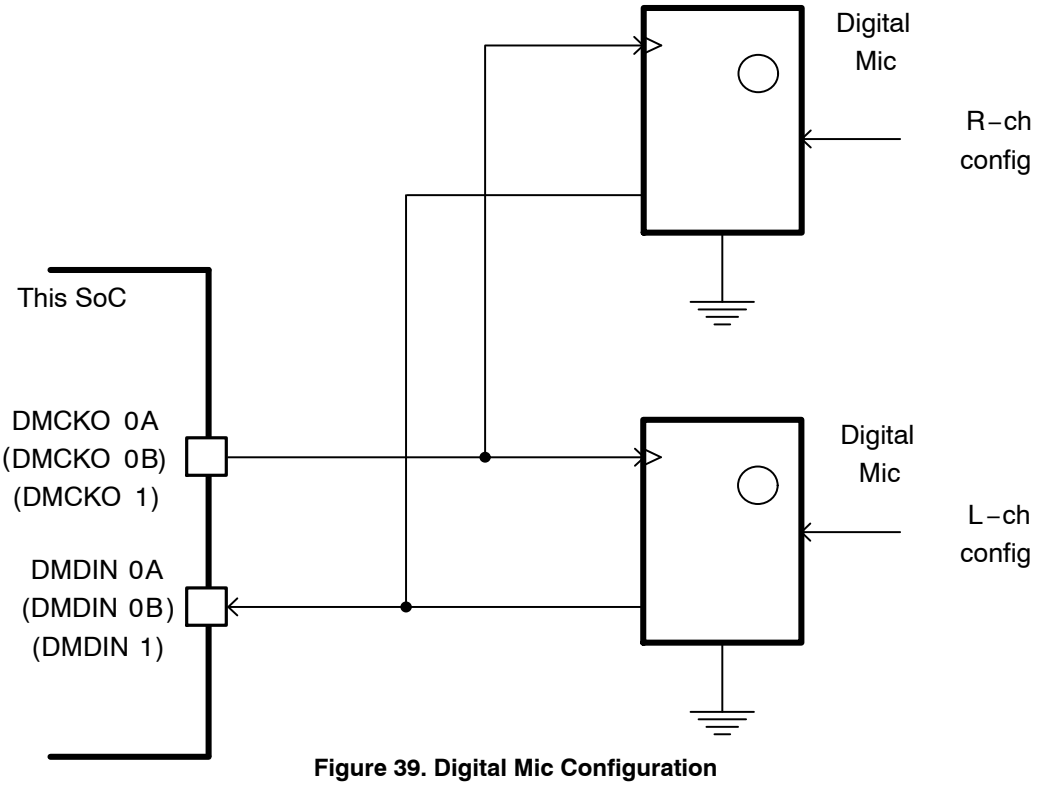


Figure 39. Digital Mic Configuration

I2C

The configuration of the I2C circuit is shown below.

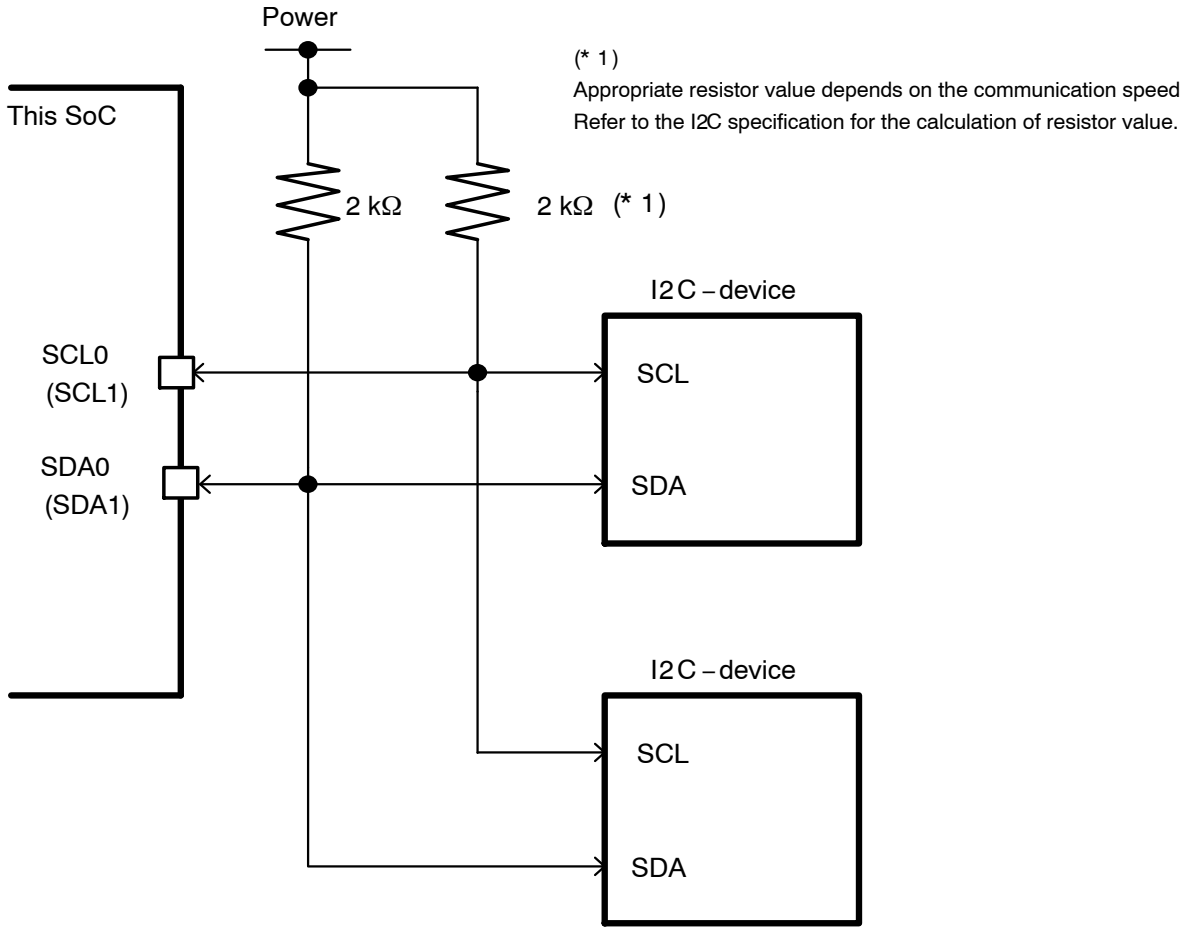


Figure 40. I2C Configuration

S−Flash I/F

The configuration of the S−Flash I/F circuit is shown below.

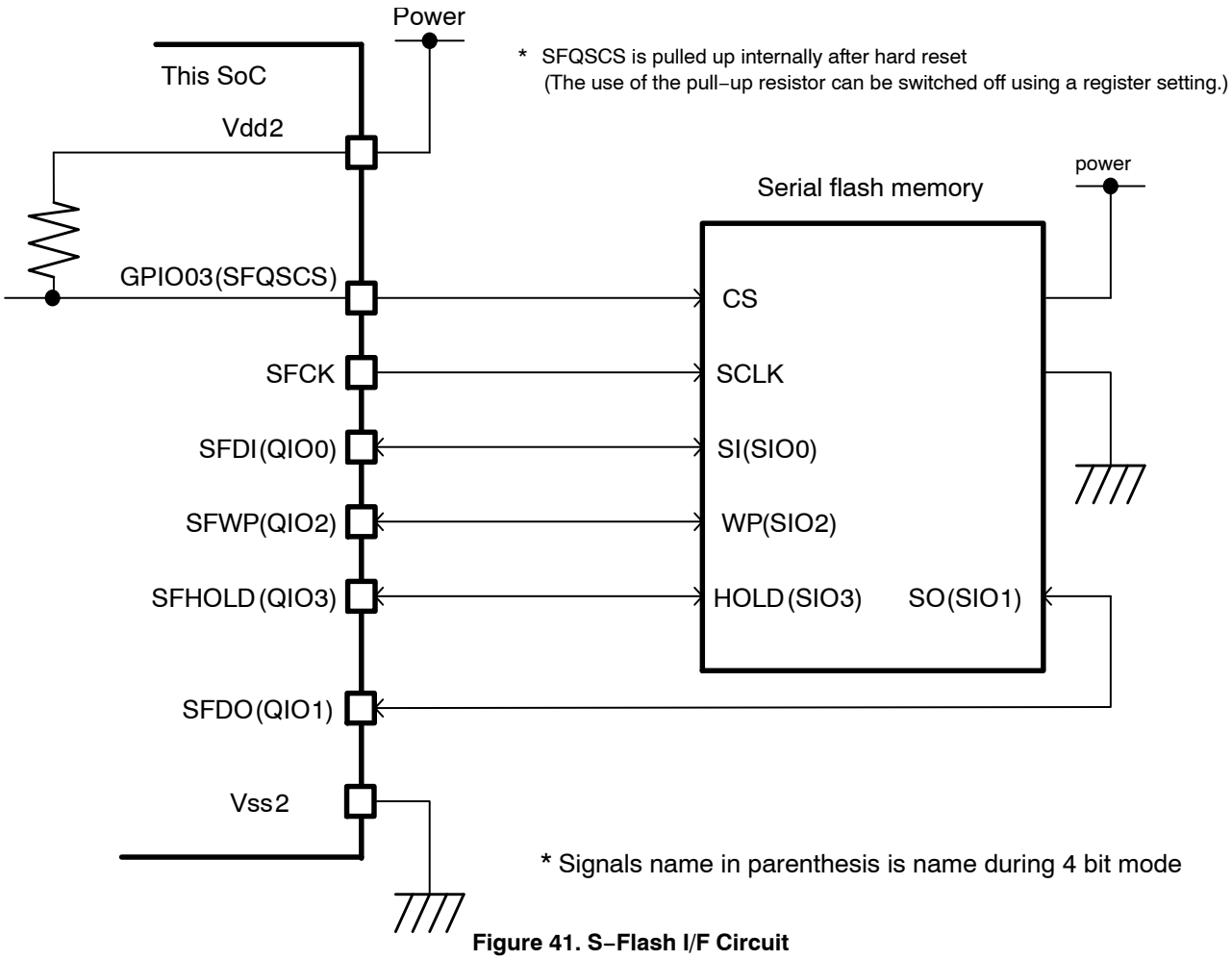


Figure 41. S−Flash I/F Circuit

RTC

The configuration of the RTC circuit is shown below.

General RTC

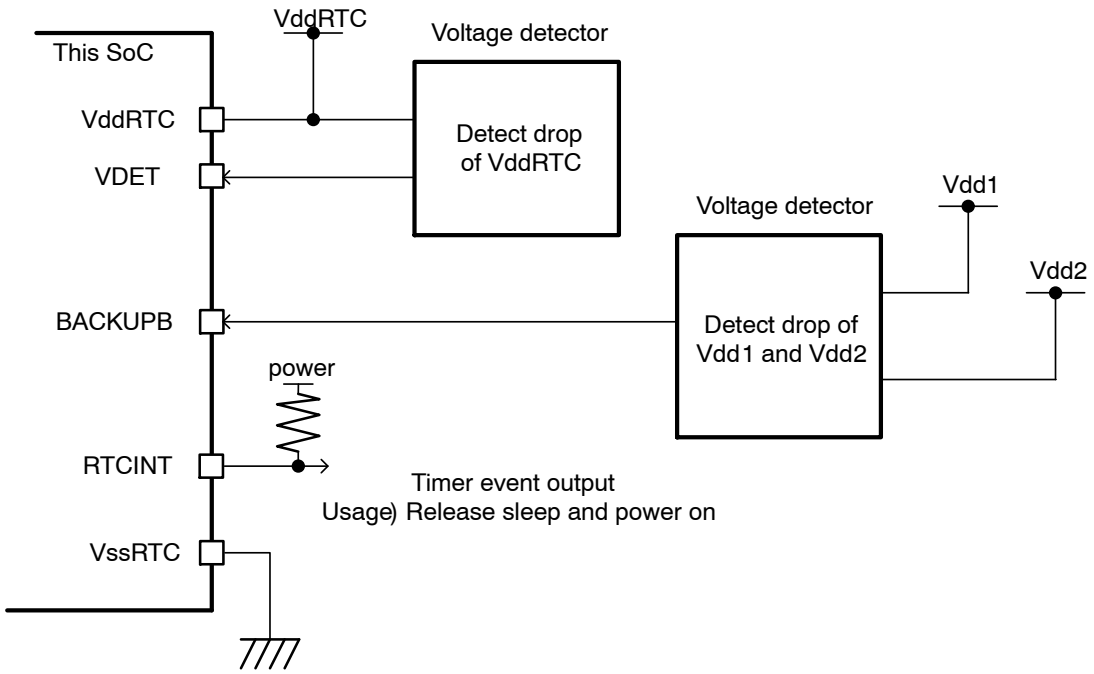
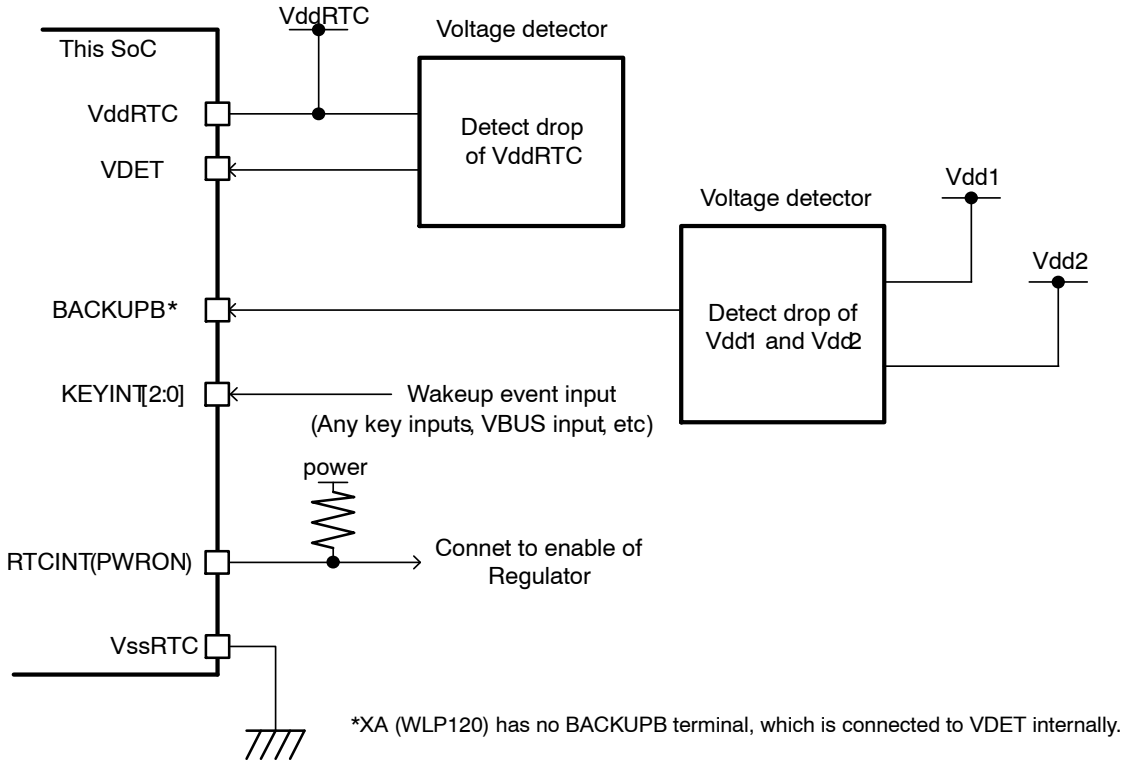


Figure 42. Configuration of the General RTC

KEYINT RTC

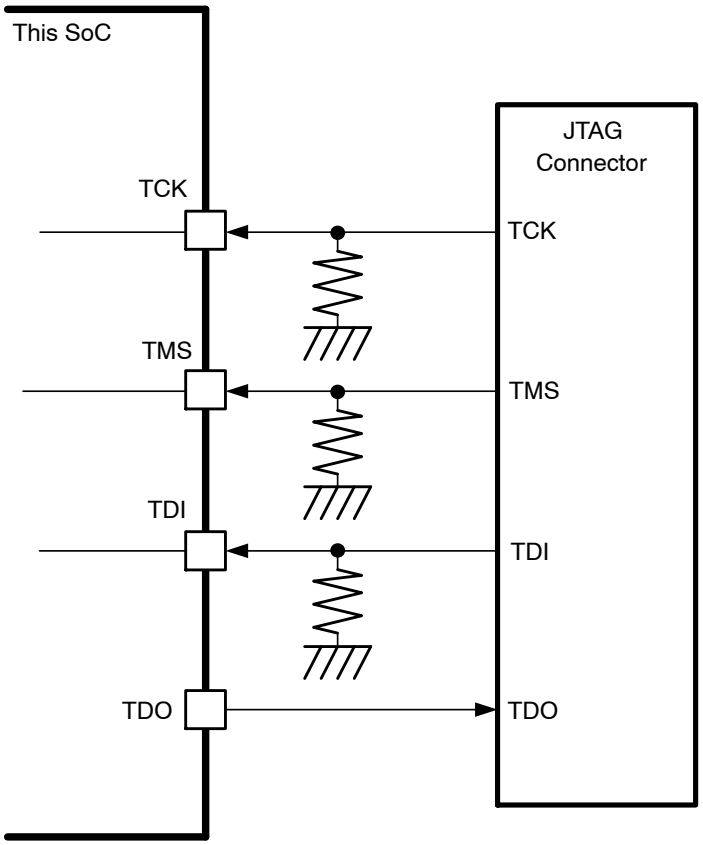


*XA (WLP120) has no BACKUPB terminal, which is connected to VDET internally.

Figure 43. Configuration of the KEYINT RTC

JTAG

The configuration of the JTAG debug circuit for LPDSP32 is shown below.



* The LPDSP32 can be reset by a JTAG software reset command issued by the debugger as well as the JTAG hardware reset signal (TRST). Therefore, the connection of the JTAG hardware reset signal between the debugger and the SoC is not mandatory.

* Internal pull down resistor can be used if they are enabled before the reset release of LPDSP 32.

* The input JTAG signals must be pulled up or down to avoid being left floating if the JTAG function is not being used.

* For further information about connecting JTAG signals, refer to the reference circuit provided by your ICE tool vendor.

Figure 44. JTAG Interface for LPDSP32

SWD

The configuration of the SWD debug circuit for Cortex−M3 is shown below.

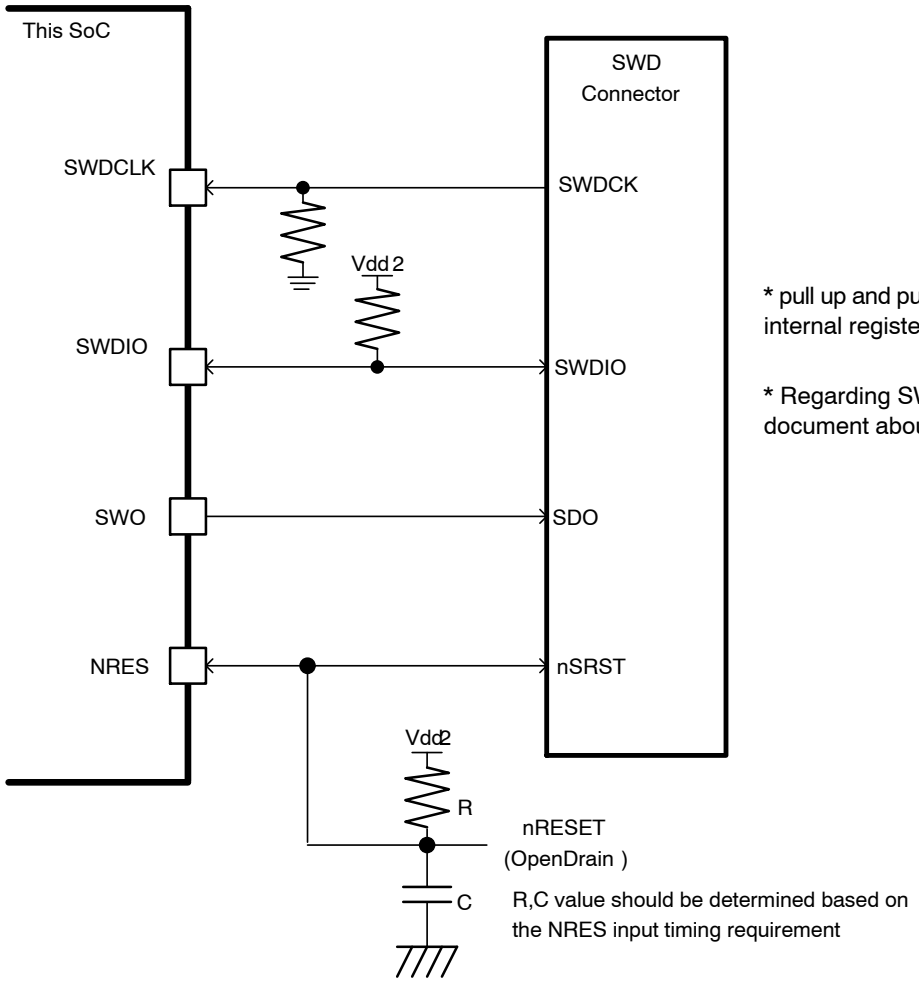
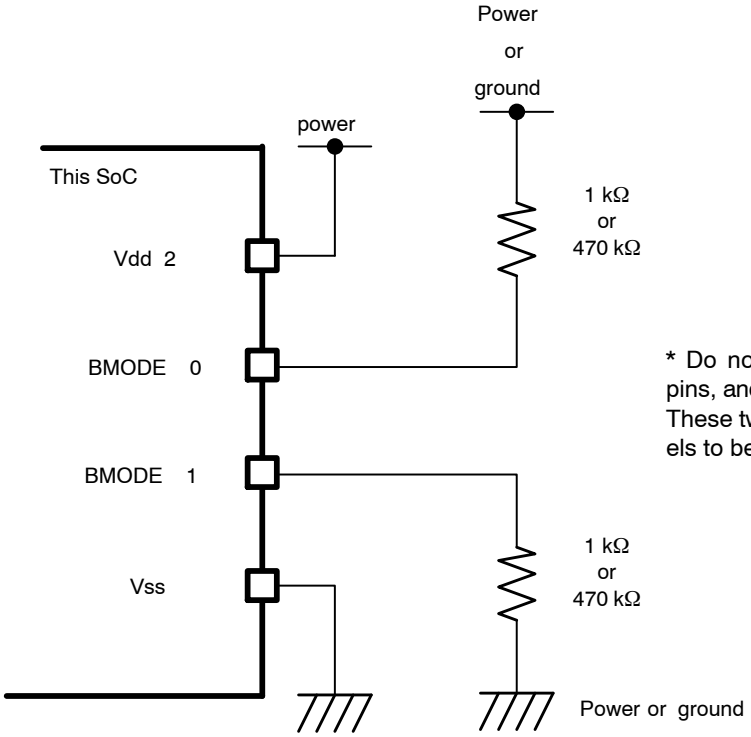


Figure 45. SWD Interface for Cortex−M3

BMODE[1: 0]

The configuration of the BMODE circuit is shown below.



* Do not connect capacitance to the BMODE pins, and avoid long wiring patterns on the board. These two factors can cause incorrect signal levels to be assigned on BMODE.

Figure 46. BMODE Configuration

POWER SUPPLY

- Don’t raise power supply steeply.
- Place bypass capacitors at each point closest to each power supply terminal, and place a power circuit at the point closest to the power supply terminals which it can supply.
- This SoC has circuits to protect from electrostatic discharge. The rush current flows in accordance with the steepness of rising curve of power supply.

INTERNAL POWER DOMAIN CONTROL

This SoC has fifteen power isolated region of internal core for leakage current reduction, these can be power supply OFF separately. Power isolated region PD−X (X means one of the fifteen region PD 1 to J) described in the table below.

Power ON / OFF for each power domain is controlled by the appropriate bit of System Controller of the power control register (LSISTBY). However, when controlling the power control register (LSISTBY), you must also control the ISOLATION control register (ISOCNT) as required. Please refer to the “System Controller” chapter in the “System Functions User’s Manual” for details.

Each power domain and its contents, along with the corresponding flags in the power control register (LSISTBY) and ISOLATION control register (ISOCNT) is as follows.

Table 57.

Name	Content	LSISTBY	ISOCNT
PD−1	Internal ROM	Bit17 STBY1	Bit17 ISOCNT1
PD-2	Internal SRAM(seg 0B)	Bit18 STBY2	Bit18 ISOCNT2
PD-3	Internal SRAM(seg 1)	Bit19 STBY3	Bit19 ISOCNT3
PD-4	Internal SRAM(seg 2)	Bit20 STBY4	Bit20 ISOCNT4
PD-5	Internal SRAM(seg 3/4)	Bit21 STBY5	Bit21 ISOCNT5
PD-6	Internal SRAM(seg 5A)	Bit22 STBY6	Bit22 ISOCNT6
PD-7	Internal SRAM(seg 5B)	Bit23 STBY7	Bit23 ISOCNT7
PD-8	Internal SRAM(seg 6)	Bit24 STBY8	Bit24 ISOCNT8
PD-9	Internal SRAM(seg 7B)	Bit25 STBY9	Bit25 ISOCNT9
PD-10	Internal SRAM(seg 7A/8/9)	Bit26 STBY10	Bit26 ISOCNT10
PD−A	Audio Block	Bit0 STBYA	Bit0 ISOCNTA
PD−E	USB 2.0 Controller SRAM	Bit4 STBYE	Bit4 ISOCNTE
PD−G	Cache for S−Flash I/F	Bit6 STBYG	Bit6 ISOCNTG
PD−H	SD Card I/F	Bit7 STBYH	Bit7 ISOCNTH
PD−J	USB 2.0 PHY	Bit9 STBYJ	Bit9 ISOCNTJ

POWER SUPPLY SEQUENCE

To ensure system stability, the power supply lines must be powered on/off in a specific sequence, based on the power supply group they are in, as described in this section.

Power Supply Groups

The power supply lines of the SoC can be grouped as follows:

1. Vdd*(Internal) – Internal core, analog power supply
   (1 V power supply)
   Vdd1, VddXT1, AVddPLL1, AVddPLL2, DVddUSBPHY1
2. Vdd*(IO) – External IO power supply
   (1.8 V / 3 V power supply)
   Vdd2, VddSD1, AVddUSBPHY2, AVddUSBPHY18, AVddADC, AVddDAMPL, AVddDAMPR
3. VddRTC – The RTC power supply
   (This is a dedicated power supply line whose on/off sequence is described separately in the next section)

Recommendation

The recommended basic sequence for powering on/off of the power supply lines is as follows. (Simultaneous power on/off is acceptable)

- Power on:
  - Vdd*(Internal) −> Vdd*(IO) −> Vsig(Signal)
- Power off:
  - Vsig(Signal) −> Vdd*(IO) −> Vdd*(Internal)

NOTE:

During power on, the sequence of Vdd*(Internal) −> Vdd*(IO) causes a SoC hard reset which prevents IO glitches. Powering on the Vdd*(IO) lines while the Vdd*(Internal) lines are powered off may generate glitches on the IO signals and the flow of through current. It is recommended that you follow the sequence above in order to avoid this. In addition, Vsig(Signal) means voltage appearance of IO signals.

In the Vdd*(IO) group, the power on sequence for the USB PHY must occur in the order AVddUSBPHY18 −> AVddUSBPHY2, while the power off sequence must occur in the order AVddUSBPHY2 −> AVddUSBPHY18.

RTC has its own dedicated power supply and power on/off sequence which is described in the following section.

RTC Terminal Control Sequence

A power supply sequence and other terminal control sequence of RTC are described as follows.

General RTC mode (RTCMODE = 1)

To power off the domains other than the RTC domain (The only RTC works), it is necessary to detect the drop in the voltage of Vdd1 and Vdd2 power supply, and set BACKUPB to Low which isolates the VddRTC Domain from the Vdd1 Domain.

Moreover, to power off the RTC domain as well, it is necessary to detect the drop in the voltage of the VddRTC power supply, and set VDET to Low. (The RTC operation stops).

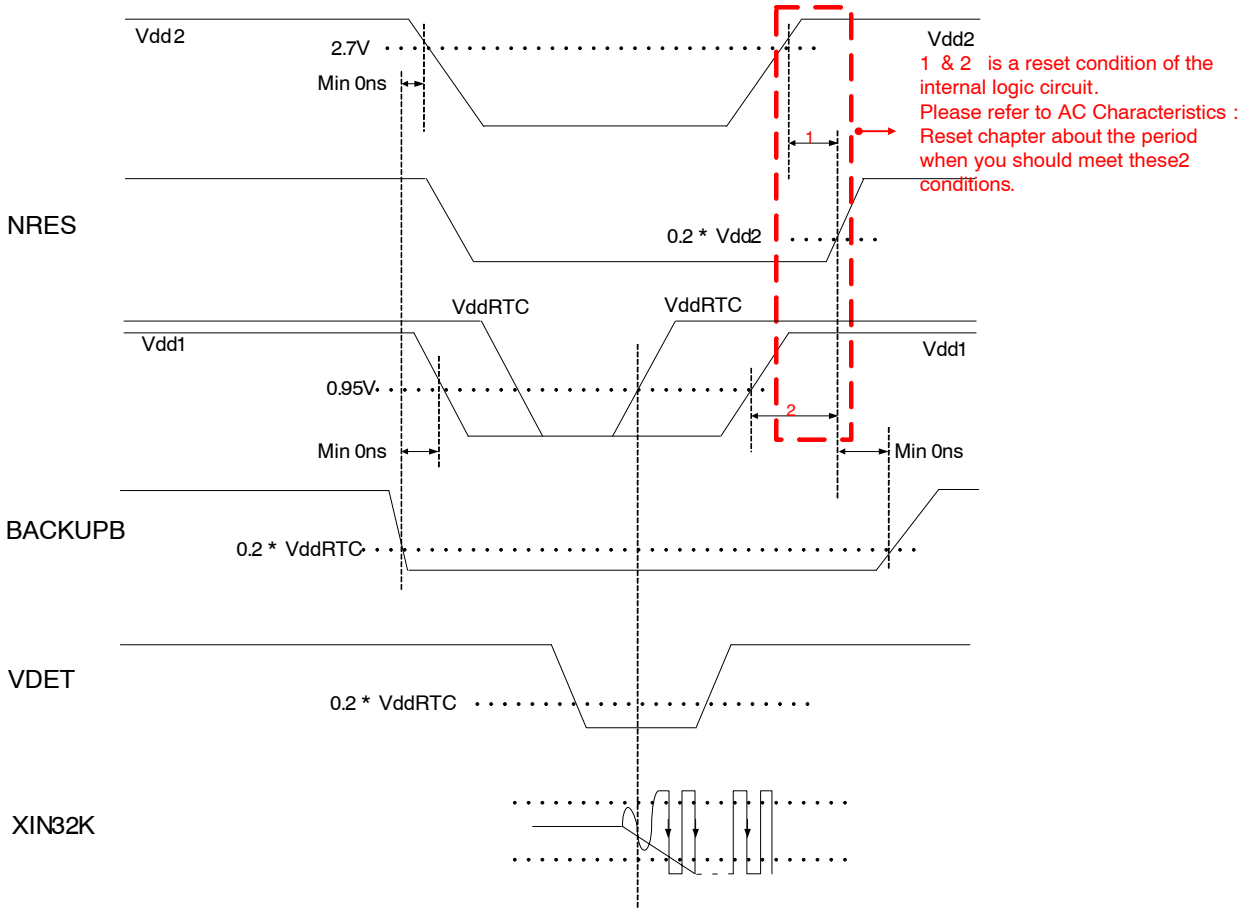


Figure 47. Timing Sequence for General RTC Mode

(Reference: Internal control logic for isolation based on BACKUPB)

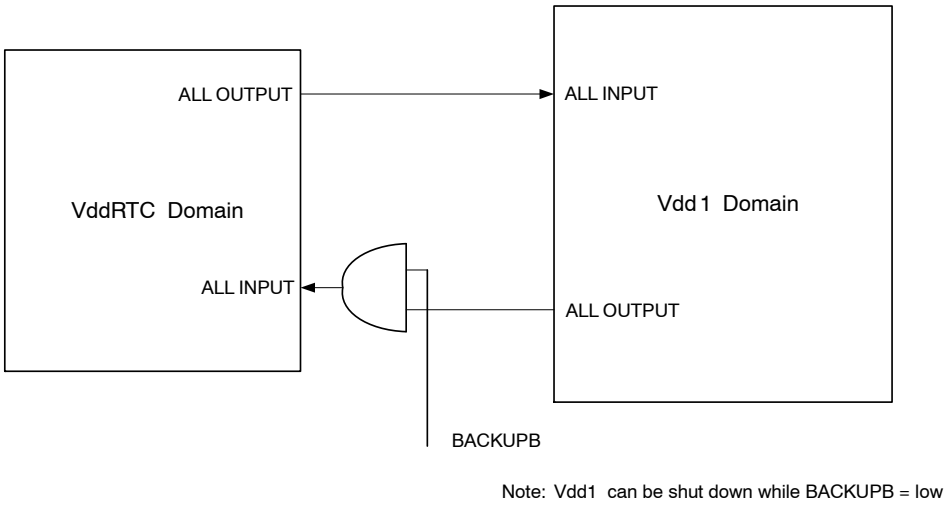


Figure 48. Internal Control Logic for Isolation

Keyint RTC Mode (RTCMODE = 0)

Using a master command from Cortex−M3, the internal sequencer of the RTC controls the operation of BACKUPB for isolation and power off. The power off sequence using the BACKUPB terminal can also be activated by an external source. Either the KEYINT input or the internal RTCINT signal can generate the power on sequence.

When powering off RTC, it is necessary to detect the drop in the voltage of the VddRTC power supply, and set VDET to Low. (The RTC operation stops).

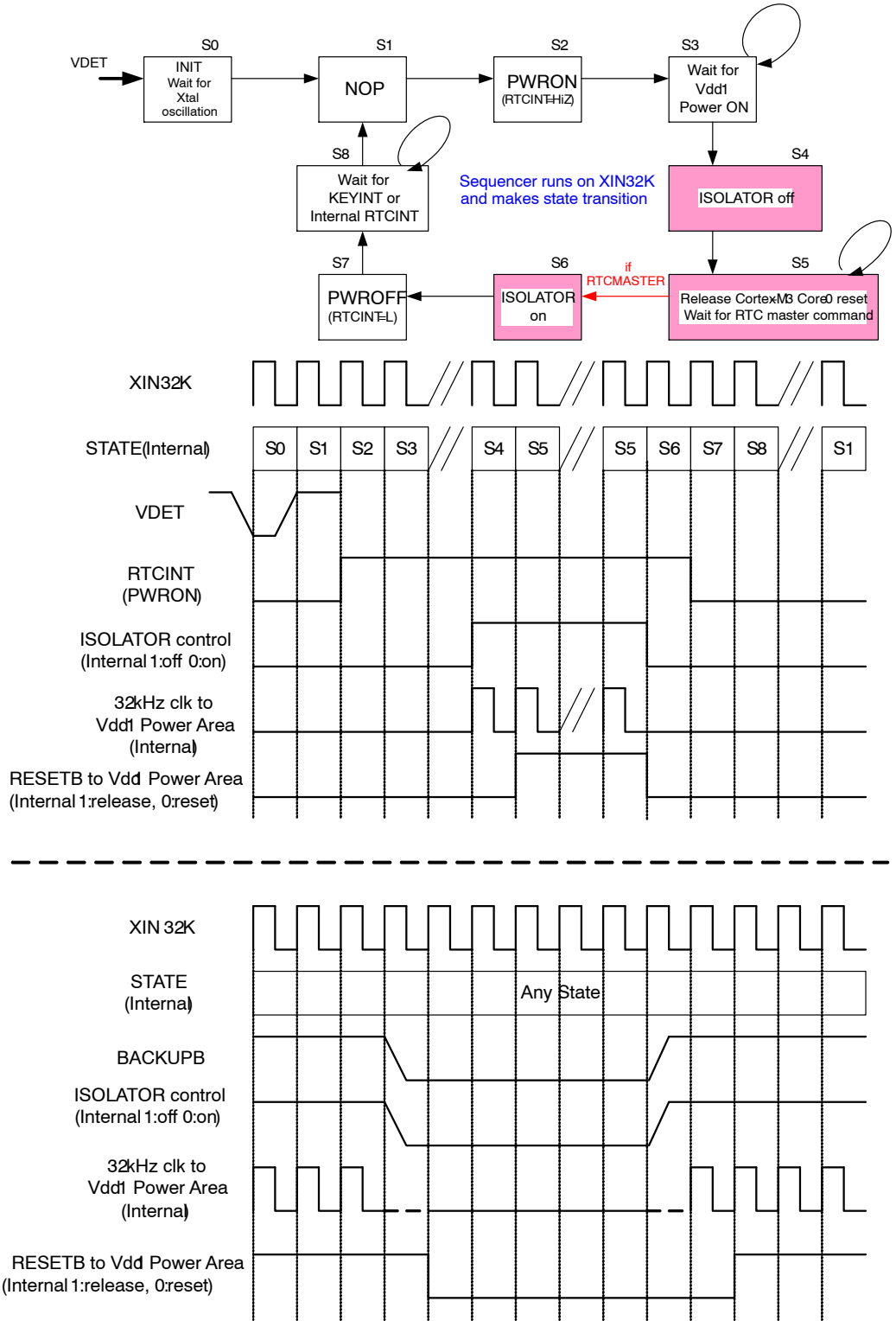


Figure 49. Timing Sequence for Keyint RTC Mode

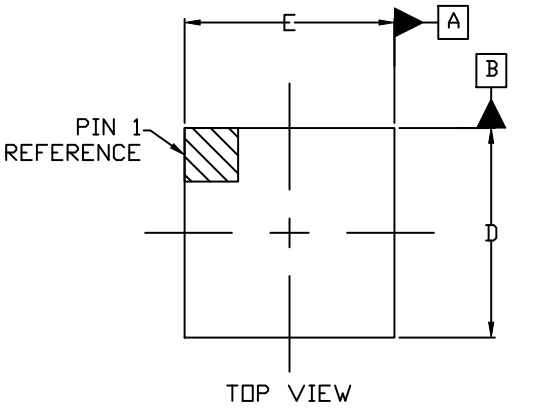
ORDERING INFORMATION

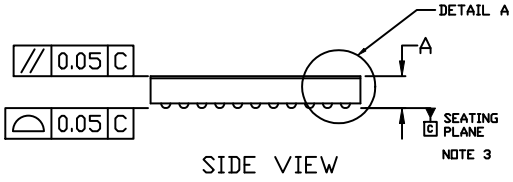
Device	Package	Shipping (Qty / Packing)†
LC823455XATBG	WLCSP120, 4.086x4.086 (Pb−Free / Halogen Free)	1000 / Tape & Reel

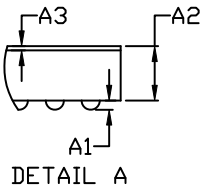
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WLCSP120, 4.086x4.086x0.62
CASE 567WG
ISSUE O

DATE 16 APR 2018



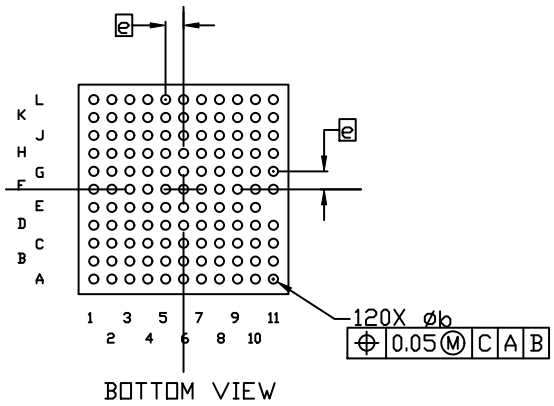


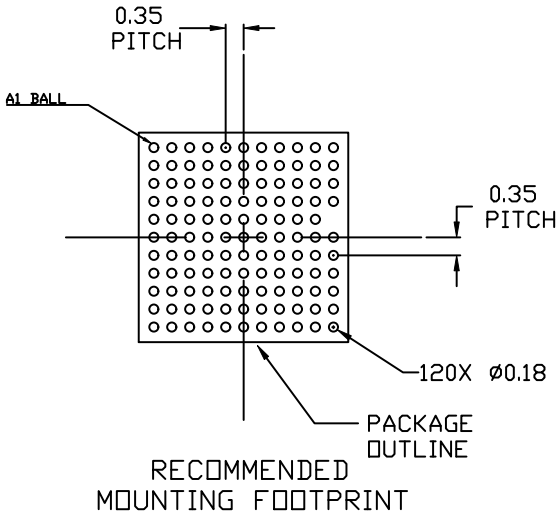


NOTES:

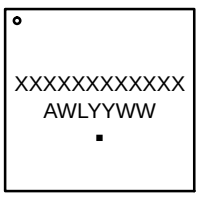
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. SEATING PLANE IS AT THE SPHERICAL CROWN SOLDER BALLS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.58	0.62	0.66
A1	0.07	0.09	0.11
A2	0.51	0.53	0.55
A3		0.04 REF	
b	0.145	0.175	0.205
D	4.056	4.086	4.116
E	4.056	4.086	4.116
e		0.35 BSC	





GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON87275G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	WLCSP120, 4.086x4.086x0.62	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊