

LC823450

低功率高分辨率音频处理系统 LSI，适用于便携式音频解决方案

说明

LC823450音频处理系统LSI，用于录制和播放音频，能够处理高分辨率32位192 kHz音频。只需使用此LSI，即可实现便携式音频所需的大部分功能。

此器件配备双CPU和DSP，具有强大的处理能力，内置1656 KB SRAM，使其可以实现大规模程序。LC823450具有集成模拟功能，可减少PCB空间和成本，还可配备各种接口，具有较高的可扩展性。此外，此器件还提供各种功能，包括DSP的SBC/AAC编解码器和用于Bluetooth®音频的UART和ASRC。虽然此器件可提供诸多功能，但采用极小的芯片尺寸，可实现低功耗，因此非常适合用于便携式音频市场(如无线耳机)，并提供高性能。

本文介绍了此LSI的特性、基本功能、电气规格、特性、应用框图以及封装尺寸。

产品特性

- 超低功耗
- ARM® Cortex®-M3 Dual Core
- 专有的32位DSP核心(LPDSP32)
- 内置大容量SRAM: 1656 KB (1.5 MB + 120 KB)
- 高分辨率32位192 kHz音频处理能力
- 为音频功能提供若干DSP代码
- 内置硬接线音频功能
MP3解码器和编码器
6波段均衡器
同步SRC、异步SRC等。
- 内置模拟模块
系统PLL、音频PLL
16位DAC、D类放大器等。
- USB2.0设备和USB2.0主机，带集成PHY
eMMC和SD卡I/F
串行闪存I/F (四路)，带高速缓冲存储器
SPI、UART、I²C等。

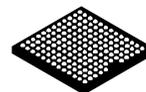
典型应用

- 录音机
- 可穿戴式音频播放器
- 蓝牙耳机
- 智能手机配件

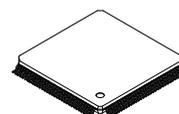


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WLCSP154
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TQFP128 / TQFP128L
CASE 932BA

ORDERING INFORMATION

See detailed ordering and shipping information on page 53 of this data sheet.

ARM®

摘要

产品特性

- Cortex-M3双核、AMBA[®] (AHB/APB)系统
 - ◆ 内置SRAM (1.5 MB)
 - ◆ 内部ROM (256 kB)。启动代码，标准功能
 - ◆ SDRAM控制器(1 * CS)
64M到256 Mbit SDRAM/移动SDRAM
 - ◆ 外部存储控制器 (2 * CS)
支持NOR FLASH、SRAM、ROM，
支持8/16位 I/F LCD控制器
提供内部ROM引导和外部存储设备引导
 - ◆ DMA控制器(8ch)
 - ◆ 中断控制器(外部90ch，内部 82ch)
 - ◆ SPI (1ch)
 - ◆ 串行闪存I/F (1ch)
四路SPI，提供缓存(16 kb，4路组关联，
128 line)功能1.8 V专用电源
 - ◆ UART (3ch)
UART1：带流量控制(CTS、RTS)
UART0\UART2：不带流量控制
 - ◆ I²C (2ch)单主机，完备/标准
 - ◆ GPIO (90ch)
 - ◆ 普通计时器，带看门狗计时器(1ch×3)
 - ◆ 多计时器(2ch×4)
 - ◆ 10位ADC (6ch)
 - ◆ SD卡I/F (3ch)
eSD/eMMC、UHS-I，不带CPRM
 - SD0：支持eSD/eMMC引导
(内部ROM引导功能) 1.8 V专用电源
 - SD1：多工，带存储器I/F
1.8 V专用电源
 - SD2：1.8 V专用电源
 - ◆ 存储器I/F (1ch)
多工，带SD1
 - ◆ USB2.0主机(HS/FS/LS)控制器、设备(HS/FS)控
制器。USB功能需要集成式PHY
Xtal (XT1)。48 MHz适用于主机，12、20、24、
48 MHz适用于不带OTG功能的设备。主机和设
备共用一个集成式PHY。

- ◆ 实时时钟
具有以下2种模式
 - 通用RTC模式：RTC (不带键输入)
 - KeyInt RTC模式：RTC (带键输入)，支持电源
开启功能
- ◆ 支持 SWD (串行线调试)，作为调试接口支持
SWV (串行线查看器)，作为跟踪接口只可跟踪
Cortex-M3双核中的一个核心。

下述功能的可用性取决于产品。

- MP3硬接线编码器/解码器
 - ◆ MP3 MPEG1、MPEG2、MPEG2.5
 - 采样率：8 kHz、11.025 kHz、12 kHz、
16 kHz、22.05 kHz、24 kHz、32 kHz、
44.1 kHz、48 kHz
 - 比特率：8 Kbps至320 Kbps
(支持Decoder-VBR)
- LPDSP32系统
 - ◆ 内部SRAM (120 k字节)
 - ◆ 内部ROM (220 k字节)
 - ◆ WMA² (Microsoft WMA Decoder Profile Level3)
 - 采样率：8 kHz、11.025 kHz、16 kHz、
22.05 kHz、32 kHz、44.1 kHz、48 kHz
 - 比特率：5 Kbps至320 Kbps (支持VBR)
 - ◆ AAC (MPEG4 LC-AAC)
 - 采样率：8 kHz、11.025 kHz、12 kHz、
16 kHz、22.05 kHz、24 kHz、32 kHz、
44.1 kHz、48 kHz
 - 比特率：8 Kbps至320 Kbps (支持VBR)
 - ◆ 可变速度控制播放(0.5至4.0倍速度)
 - WMA和AAC最高可以2.0倍速¹播放
 - PCM最高可以4.0倍速度播放
 - MP3 (带硬接线解码器)最高可以4.0倍速度播放
 - ◆ 噪声消除器等。
 - ◆ JTAG ICE

¹ MPEG Layer-3 audio coding technology licensed from Fraunhofer IIS and Thomson.

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- 支持蓝牙协议栈³
- 支持其他音频功能
 - ◆ 6波段均衡器(EQ3)
 - ◆ 音量、静音
 - ◆ 电平表
 - ◆ 音频计时器，带中断发生器
 - ◆ 16/24/32位192 kHz PCM I/F (2ch×2)。主/从，I²S
 - ◆ SSRC (同步采样率转换器)转换范围：0.25至64
 - ◆ ASRC (异步采样率转换器)
可减少抖动，支持USB音频类和蓝牙串流
 - ◆ 蜂鸣声发生器
 - ◆ 数字麦克风I/F (2ch×1)
 - ◆ 16位音频DAC (2ch)，带D类放大器，适用于头戴式耳机(2ch)。需要外部LC LPF
- 音频时钟发生器
 - ◆ 音频专用PLL (集成PLL2:1 V和PLL3:3 V)
 - ◆ 可选择PLL参考时钟
XT1 (1到50 MHz主xtal)
XTRTC (32.768 kHz RTC xtal)
PCM I/F MCLK0 (/MCLK1)、BCK0、BCK1
- 电源
 - ◆ 典型电压
 - LOGIC(Vdd1)、XT1(VddXT1)、
PLL1(AVddPLL1)、PLL2(AVddPLL2) = 1.0 V
 - PLL3(AVddPLL3) = 3.3 V
 - RTC(VddRTC) = 1.0 V
 - I/O(Vdd2) = 1.8 V或3.3 V
 - SD0(VddSD0) = 1.8 V或3.3 V
 - SD1(VddSD1) = 1.8 V或3.3 V
 - SD2(VddSD2) = 1.8 V或3.3 V
 - 串行闪存I/F(VddQSPI) = 1.8 V或3.3 V
 - ADC(AVddADC) = 3.3 V
 - USB PHY1(AVddUSBPHY1、DVddUSBPHY1)
= 1.0 V (不带USB接口)或1.2 V (带USB接口)
 - USB PHY2(AVddUSBPHY2) = 2.8 V (不带USB
接口)或3.3 V (带USB接口)
 - D类放大器(AVddDAMPL、AvddDAMPR) =
1.2 V

³ The product name for which Bluetooth Protocol Stack is available is determined. Please contact our representative for license fee for the Stack.
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封装代码和功能差异

封装代码="RA"的产品正在规划中

Table 1. FUNCTIONAL DIFFERENCE

Function	Package Code			
	TA	XA, XC	XB, XD	RA
Package	TQFP128L	WLP154		XBGA240
Cortex-M3 Dual Core	Single	Single	Dual	Dual
SDRAM Controller				Available
External Memory Controller		8bit I/F (LCD I/F, etc.)	8bit I/F (LCD I/F, etc.)	Available
SD2	Available		Available	Available
10bit ADC Conversion Speed	MAX 5 MHz (Note 2)			MAX 20 MHz (Note 4)
10bit ADC Reference Voltage	VRH=AvddADC VRL=AVssADC (Note 3)			VRH=AVddADC and lower VRL=AVssADC and higher
PCM1(PCM I/F ch1)	BCK1/LRCK1 share pins with other function	Available	Available	Available
MP3 Hard Wired Encoder	Available		Available	Available
16bit Audio DAC, Class-D AMP	Available		Available	Available
PLL2(1 V PLL) PLL3(3 V PLL)	Only PLL2	Available	Available	Only PLL2
XTALINFO[1:0] Input	"00" (24 MHz)	Available	Available	Available
RTCMODE Input	"1" (General RTC mode)	Available	Available	Available
KEYINT[2:0] Input		Available	Available	Available
External Interrupt	45 ch	61 ch	61 ch	90 ch
GPIO	45 ch	61 ch	61 ch	90 ch

1. Pin shared for multiple function. Refer to Terminal Functions for details.
2. Intentionally not used.
3. VR is open inside.
4. VRH = AvddADC, VRL = AVssADC inside.
5. Decoupling capacitor is required MAX 5 MHz in case of open.

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框图

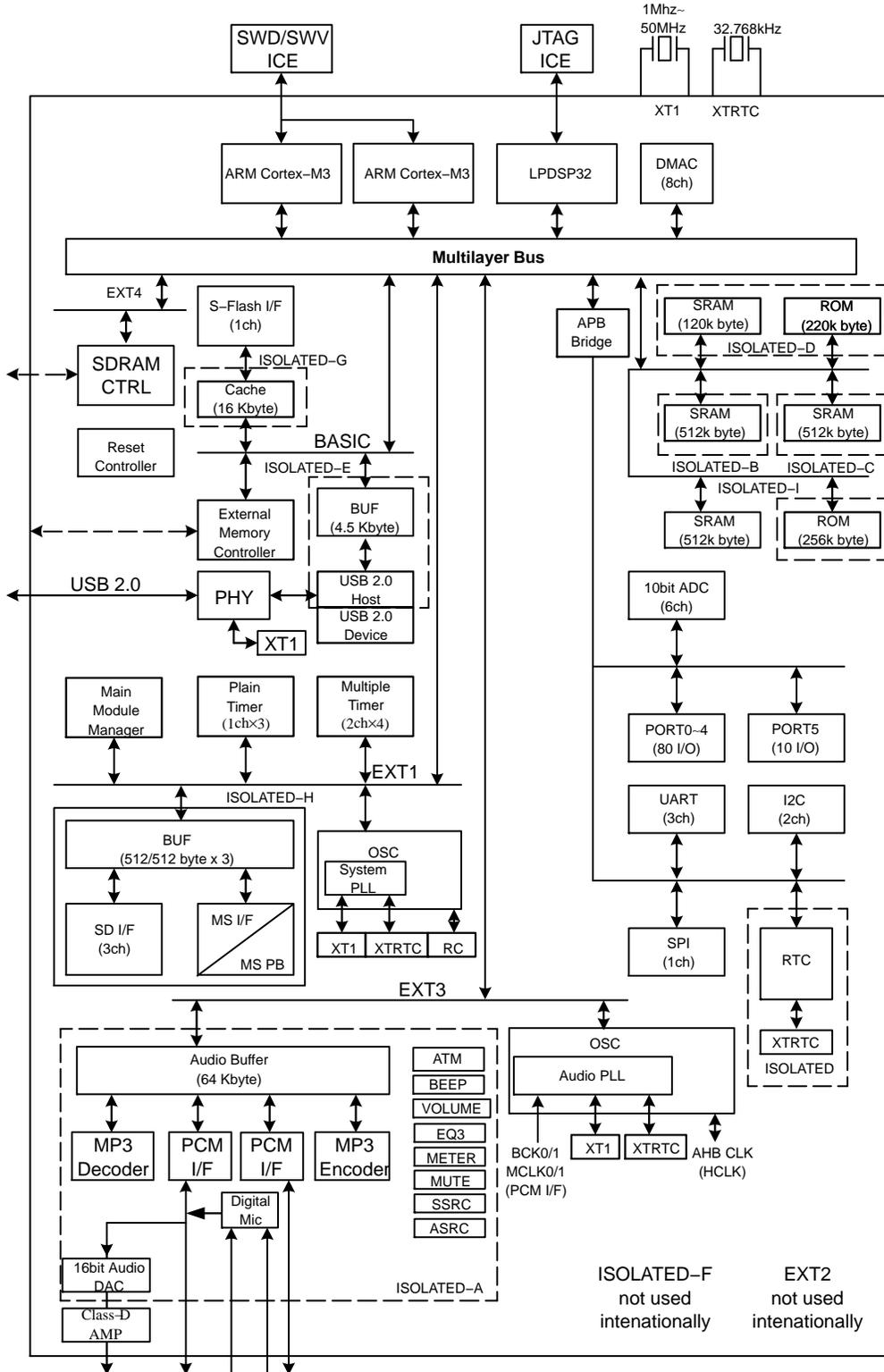


Figure 1. Top

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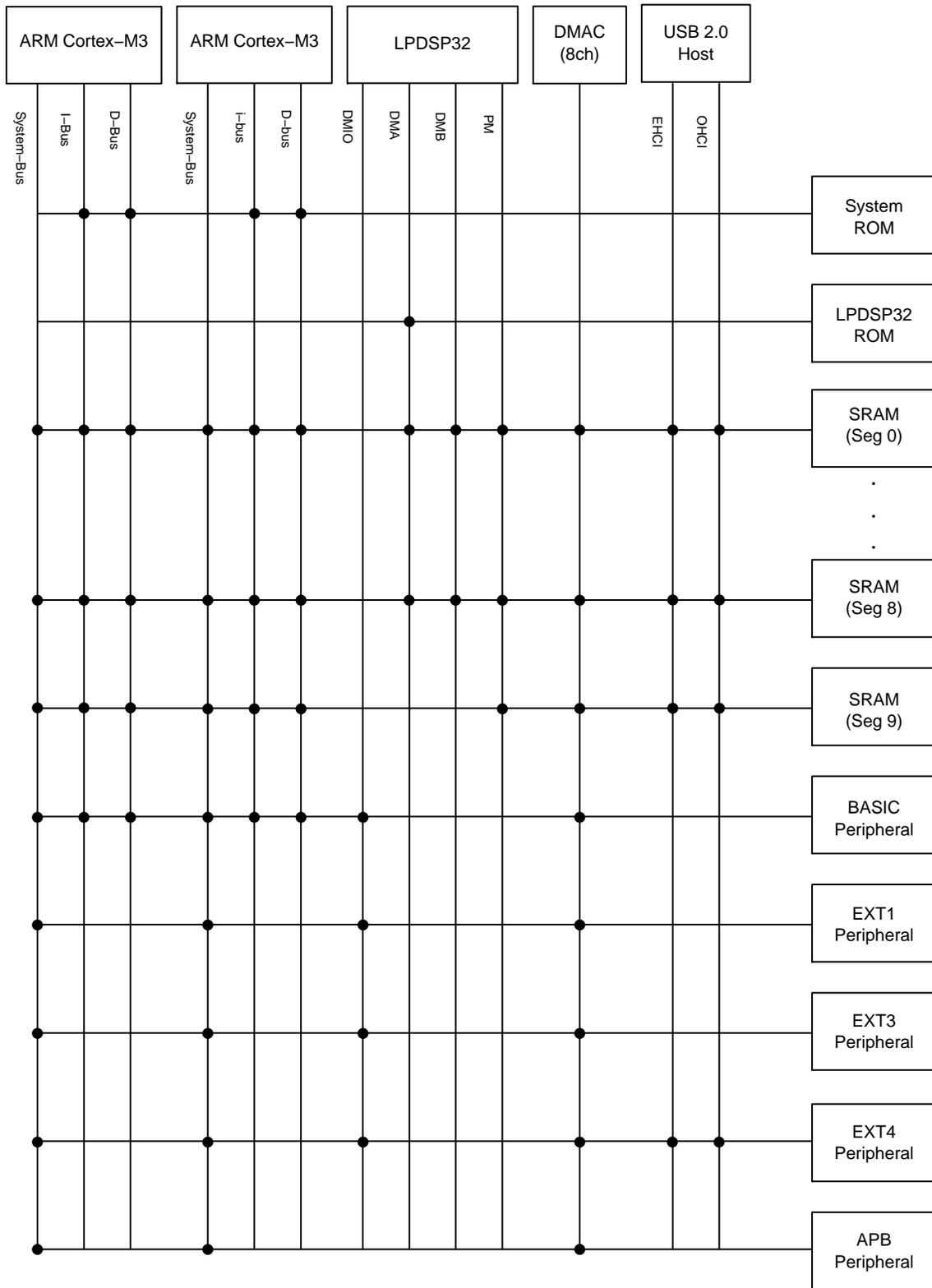


Figure 2. Bus Matrix

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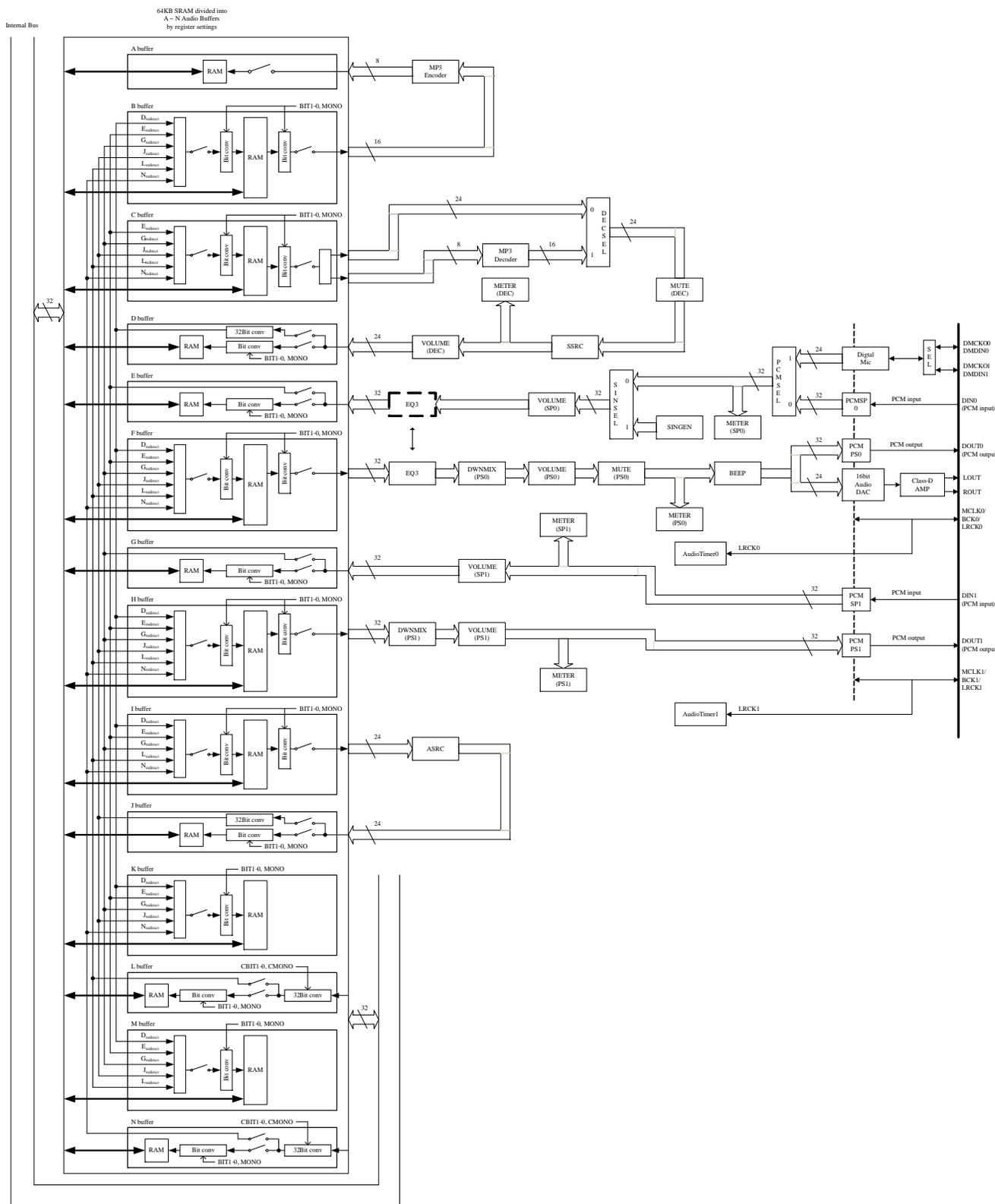


Figure 3. Audio

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端子功能

TA:封装代码="TA"
 XA:封装代码="XA"
 XB:封装代码="XB"

XC:封装代码="XC"
 XD:封装代码="XD"

Table 2. JTAG/SWD

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)		
					TA	XA,XC	XB,XD
TDO	-	O	JTAG test data outputSD	VddSD1	○	○	○
SDWP1	Pos	I	SD I/F Ch1 write protect		○	○	○
INS	Neg	I	Memory Stick INS		○	○	○
GPIO21	-	B	GPIO		○	○	○
EXTINT21	-	I	External Interrupt 2-bit1		○	○	○
TDI	-	I	JTAG test data input	VddSD1	○	○	○
SDCD1	Neg	I	SD I/F Ch2 write protect		○	○	○
SWO	-	O	Serial wire view data		○	○	○
GPIO20	-	B	GPIO		○	○	○
EXTINT20	-	I	External Interrupt 2-bit0		○	○	○
TMS	-	I	JTAG test data select	VddSD2	○	○	○
SDWP2	Pos	I	SD I/F Ch2 write protect		○	(Note 6)	○
GPIO28	-	B	GPIO		○	○	○
EXTINT28	-	I	External Interrupt 2-bit8		○	○	○
TCK	Pos	I	JTAG test clock	VddSD2	○	○	○
SDCD2	Neg	I	SD I/F Ch2 detect		○	(Note 6)	○
GPIO29	-	B	GPIO		○	○	○
EXTINT29	-	I	External Interrupt 2-bit9		○	○	○
SWDCLK	Pos	I	Serial wire clock	Vdd2	○	○	○
DMCKO1	-	O	Digital MicCh1Clock Output		○	○	○
GPIO58	-	B	GPIO		○	○	○
EXTINT58	-	I	External Interrupt 5-bit8		○	○	○
SWDIO	-	B	Serial wire Data	Vdd2	○	○	○
DMDIN1	-	I	Digital MicCh1 Data Input		○	○	○
GPIO59	-	B	GPIO		○	○	○
EXTINT59	-	I	External Interrupt 5-bit9		○	○	○
Sum					6	6	6

RTC

XIN32K	Pos	I	32.768 kHz XTAL Input (XTRTC)	Vdd2	○	○	○
XOUT32K	-	O	32.768 kHz XTAL Output (XTRTC)		○	○	○
VDET	Neg	I	RTC power detect Input		○	○	○
RTCINT	Neg	O	RTC Interrupt Output (Normal:HiZ, Interrupt enabled: Low Output)		○	○	○
BACKUPB	Neg	I	RTC backup mode input	Vdd2	○	○	○

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Table 2. JTAG/SWD (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)		
Multiplexed Function					TA	XA,XC	XB,XD
RTC							
KEYINT[2:0]	–	I	RTC KEY input can be used when KeyInt RTC mode	Vdd2	○	○	○
RTCMODE	–	I	RTC mode input (Note 7) Set General RTC or KeyInt RTC mode RTCMODE = G “0”: KeyInt RTC mode G “1”: General RTC mode Bonding internally for “TA” product	Vdd2	○	○	○
VddRTC	–	P	RTC power supply	Vdd2	○	○	○
VssRTC	–	P	RTC ground	Vdd2	○	○	○
Sum					7	11	11
EXTERNAL INTERRUPT/GPIO							
SDRADDR12	–	O	SDRAM address	Vdd2			
GPIO2A	–	B	GPIO				
EXTINT2A	–	I	External Interrupt 2–bit10				
SCL1	–	O	I ² C ch1 Clock (open drain output)	Vdd2	○	○	○
GPIO2B	–	B	GPIO		○	○	○
EXTINT2B	–	I	External Interrupt 2–bit11		○	○	○
SDA1	–	B	I ² C ch1 Clock (open drain output)	Vdd2	○	○	○
GPIO2C	–	B	GPIO		○	○	○
EXTINT2C	–	I	External Interrupt 2–bit12		○	○	○
SDRADDR11	–	O	SDRAM address	Vdd2			
DMCKO0	–	O	Digital Mic Clock Ch0 Output		○	○	○
GPIO2D	–	B	GPIO		○	○	○
EXTINT2D	–	I	External Interrupt 2–bit13	Vdd2	○	○	○
EXTINT2E	–	I	External Interrupt 2–bit14		○	○	○
GPIO2E	–	B	GPIO *While Internal ROM boot, this terminal is used as boot monitor signal.		○	○	○
EXTINT2F	–	I	External Interrupt 2–bit14	Vdd2	○	○	○
GPIO2F	–	B	GPIO *While Internal ROM boot, this terminal is used as boot monitor signal.		○	○	○
Sum					5	5	5
SPI (SERIAL I/F CH0)/S-FLASH I/F (SERIAL I/F CH1)							
SCK0	Neg	B	Serial I/F Ch0 Clock	Vdd2	○	○	○
GPIO1D	–	B	GPIO		○	○	○
EXTINT1D	–	I	External Interrupt 1–bit13		○	○	○
SDI0	–	I	Serial I/F Ch0 Data Input	Vdd2	○	○	○
GPIO1E	–	B	GPIO		○	○	○
EXTINT1E	–	I	External Interrupt 1–bit14		○	○	○

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Table 2. JTAG/SWD (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)		
Multiplexed Function					TA	XA,XC	XB,XD
SPI (SERIAL I/F CH0)/S-FLASH I/F (SERIAL I/F CH1)							
SDO0	–	O	Serial I/F Ch0 Data Output	Vdd2	○	○	○
GPIO1F	–	B	GPIO		○	○	○
EXTINT1F	–	I	External Interrupt 1–bit15		○	○	○
SCK1	Neg	O	Serial I/F Ch1 Clock (QSPI Clock)	VddQSPI			
GPIO0D	–	B	GPIO		○	○	○
EXTINT0D	–	I	External Interrupt 0 bit13		○	○	○
SDI1(QIO0)	–	O(B)	Serial I/F Ch1 Data Input (QSPI Data 1)	VddQSPI	○	○	○
GPIO0E	–	B	GPIO		○	○	○
EXTINT0E	–	I	External Interrupt 0–bit14		○	○	○
SDO1(QIO1)	–	I(B)	Serial I/F Ch1 Data Input (QSPI Data 1)	VddQSPI	○	○	○
GPIO0F	–	B	GPIO		○	○	○
EXTINT0F	–	I	External Interrupt 0–bit15		○	○	○
SWP1(QIO2)	Neg	O(B)	Serial I/F Ch1 write protect (QSPI Data 2)	VddQSPI	○	○	○
GPIO11	–	B	GPIO		○	○	○
EXTINT11	–	I	External Interrupt 1–bit1		○	○	○
SHOLD1(QIO3)	Neg	O(B)	Serial I/F Ch1 hold (QSPI Data 3)	VddQSPI	○	○	○
GPIO12	–	B	GPIO		○	○	○
EXTINT12	–	I	External Interrupt 1–bit2		○	○	○
Sum					8	8	8
I²C							
SCL0	–	O	I ² C ch0 Clock (open drain output)	Vdd2	○	○	○
GPIO07	–	B	GPIO		○	○	○
EXTINT07	–	I	External Interrupt 0–bit7		○	○	○
SDA0	–	B	I ² C ch0 Data (open drain output)	Vdd2	○	○	○
GPIO08	–	B	GPIO		○	○	○
EXTINT08	–	I	External Interrupt 0–bit8		○	○	○
Sum					2	2	2
UART							
TXD1	–	O	UART Ch1 transmit Data	VddSD2	○	○	○
SDAT20	–	B	SD I/F Ch2 Data 0		○	(Note 6)	○
GPIO04	–	B	GPIO		○	○	○
EXTINT04	–	I	External Interrupt 0–bit4		○	○	○
RXD1	–	I	UART Ch1 receive Data	VddSD2	○	○	○
SDAT21	–	B	SD I/F Ch2 Data 1		○	(Note 6)	○
GPIO05	–	B	GPIO		○	○	○
EXTINT05	–	I	External Interrupt 0–bit5		○	○	○

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Table 2. JTAG/SWD (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)		
Multiplexed Function					TA	XA,XC	XB,XD

UART

CTS1	Neg	I	UART Ch1 clear to send	VddSD2	○	○	○
SDAT22	–	B	SD I/F Ch2 Data 2		○	(Note 6)	○
RXD0	–	I	UART Ch0 receive Data		○	○	○
GPIO56	–	B	GPIO		○	○	○
EXTINT56	–	I	External Interrupt 5–bit6		○	○	○
RTS1	Neg	O	UART Ch1 request to send	VddSD2	○	○	○
SDAT23	–	B	SD I/F Ch2 Data 3		○	(Note 6)	○
TXD0	–	O	UART Ch0 transmit Data		○	○	○
GPIO57	–	B	GPIO		○	○	○
EXTINT57	–	I	External Interrupt 5–bit7		○	○	○
TXD2	–	O	UART Ch2 transmit Data	VddQSPI	○	○	○
TIOCA10	–	B	MTM1 Ch0A – target signal of pulse–length–reader function – output of sentinel–inform–function – output of PWM output		○	○	○
GPIO0B	–	B	GPIO		○	○	○
EXTINT0B	–	I	External Interrupt 0–bit11		○	○	○
RXD2	–	I	UART ch2 receive Data	VddQSPI	○	○	○
TIOCA11	–	B	MTM1 Ch1A – target signal of pulse–length–reader function – output of sentinel–inform–function – output of PWM output		○	○	○
GPIO0C	–	B	GPIO		○	○	○
EXTINT0C	–	I	External Interrupt 0–bit12		○	○	○
Sum					6	6	6

TIMER

TIOCA00	–	B	MTM0 Ch0A – target signal of pulse–length–reader function – output of sentinel–inform–function – output of PWM output	VddSD2	○	○	○
SDCLK2	–	O	SD I/F Ch2 Clock Output		○	(Note 6)	○
PHI0	–	O	System Clock Output 0		○	○	○
GPIO09	–	B	GPIO		○	○	○
EXTINT09	–	I	External Interrupt 0–bit9		○	○	○

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Table 2. JTAG/SWD (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)		
					TA	XA,XC	XB,XD
TIMER							
TIOCA01	–	B	MTM0 Ch1A – target signal of pulse-length–reader function – output of sentinel–inform–function – output of PWM output	VddSD2	○	(Note 6)	○
SDCMD2	–	B	SD I/F Ch2 command line		○	○	○
PHI1	–	O	System Clock Output 1		○	○	○
GPIO0A	–	B	GPIO		○	○	○
EXTINT0A	–	I	External Interrupt 0–bit10		○	(Note 6)	○
TIOCB00	–	B	MTM0 Ch0B – target signal of pulse-length–reader function – output of sentinel–inform–function	Vdd2	○	○	○
DIN1	–	I	PCM1 Data Input		○	○	○
DMDIN0	–	I	Digital Mic Data Ch0 Input		○	○	○
GPIO02	–	B	GPIO		○	○	○
EXTINT02	–	I	External Interrupt 0–bit2		○	(Note 6)	○
TIOCB01	–	B	MTM0 Ch1B – target signal of pulse-length–reader function – output of sentinel–inform–function	VddQSPI	○	○	○
DMCKO0	–	O	Digital Mic Clock Ch0 Output		○	○	○
QSCS	Neg	O	Serial I/Fch1 QSPI chip select *While Serial Flash Boot, this is used as chip select of Serial Flash		○	○	○
GPIO03	–	B	GPIO		○	○	○
EXTINT03	–	I	External Interrupt 0–bit3		○	○	○
TCLKA0	–	I	MTM0 external Clock A	Vdd2	○	○	○
BCK1	–	B	PCM1 bit Clock		○	○	○
GPIO00	–	B	GPIO		○	○	○
EXTINT00	–	I	External Interrupt 0–bit0		○	○	○
TCLKB0	–	I	MTM0 external Clock B	Vdd2	○	○	○
LRCK1	–	B	PCM1 LR Clock		○	○	○
GPIO01	–	B	GPIO		○	○	○
EXTINT01	–	I	External Interrupt 0–bit1		○	○	○
Sum					6	6	6
PCM I/F							
MCLK0	Pos	B	PCM0 master Clock	Vdd2	○	○	○
MCLK1	Pos	B	PCM1 master Clock		○	○	○
GPIO18	–	B	GPIO		○	○	○
EXTINT18	–	I	External Interrupt 1–bit8		○	○	○

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Table 2. JTAG/SWD (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)		
Multiplexed Function					TA	XA,XC	XB,XD
PCM I/F							
BCK0	–	B	PCM0 bit Clock	Vdd2	○	(Note 6)	○
DMCKO1	–	O	Digital Mic Ch1 Clock Output		○	○	○
GPIO19	–	B	GPIO		○	○	○
EXTINT19	–	I	External Interrupt 1–bit9		○	○	○
LRCK0	–	B	PCM0 LR Clock	Vdd2	○	○	○
DMDIN1	–	I	Digital Mic ch1 Data Input		○	(Note 6)	○
GPIO1A	–	B	GPIO		○	○	○
EXTINT1A	–	I	External Interrupt 1–bit10		○	○	○
DIN0	–	I	PCM0 Data Input	Vdd2	○	○	○
DMDIN0	–	I	Digital Mic Ch0 Data Input		○	○	○
GPIO1B	–	B	GPIO		○	○	○
EXTINT1B	–	I	External Interrupt 1–bit11		○	○	○
DOUT0	–	O	PCM0 Data Output	Vdd2	○	○	○
DMCKO0	–	O	Digital Mic Ch0 Data Input		○	○	○
GPIO1C	–	B	GPIO		○	○	○
EXTINT1C	–	I	External Interrupt 1–bit12		○	○	○
BCK1	–	B	PCM1 bit Clock	Vdd2		○	○
GPIO13	–	B	GPIO			○	○
EXTINT13	–	I	External Interrupt 1–bit3			○	○
LRCK1	–	B	PCM1 LR Clock	Vdd2		○	○
GPIO14	–	B	GPIO			○	○
EXTINT14	–	I	External Interrupt 1–bit4			○	○
DOUT1	–	O	PCM1 Data Output	Vdd2	○	○	○
GPIO15	–	B	GPIO		○	○	○
EXTINT15	–	I	External Interrupt 1–bit5		○	○	○
Sum					6	8	8
SD I/F/MS I/F							
SDCLK0	–	O	SD I/F Ch0 Clock Output	VddSD0	○	○	○
SDCMD0	–	B	SD I/F Ch0 command line		○	○	○
SDAT0[3:0]	–	B	SD I/F Ch0 Data		○	○	○
SDCLK1	–	O	SD I/F Ch1 Clock Output		○	○	○
SCLK	–	O	Memory Stick Clock Output	VddSD0	○	○	○
GPIO22	–	B	GPIO		○	○	○
EXTINT22	–	I	External Interrupt 2–bit2		○	○	○
SDCMD1	–	B	SD I/F Ch1 command line	VddSD1	○	○	○
BS	–	O	Memory Stick BS		○	○	○
GPIO23	–	B	GPIO		○	○	○

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Table 2. JTAG/SWD (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)		
Multiplexed Function					TA	XA,XC	XB,XD
SD IF/MS IF							
EXTINT23	–	I	External Interrupt 2–bit3	VddSD1	○	○	○
SDAT1[3:0]	–	B	SD I/F Ch1 Data		○	○	○
DATA[3:0]	–	B	Memory Stick Data		○	○	○
GPIO2[7:4]	–	B	GPIO	VddSD1	○	○	○
EXTINT2[7:4]	–	I	External Interrupt 2–bit7 to bit4		○	○	○
Sum					12	12	12
SDRAM I/F							
SDRCLK	Neg	O	SDRAM Clock Output	Vdd2			
SDRCKE	Pos	O	SDRAM Clock enable Output	Vdd2			
SDRCS	Neg	O	SDRAM chip select Output	Vdd2			
SDRWE	Neg	O	SDRAM write enable Output	Vdd2			
SDRCAS	Neg	O	SDRAM CAS Output	Vdd2			
SDRRAS	Neg	O	SDRAM RAS Output	Vdd2			
SDRDQM[1:0]	Pos	O	SDRAM Data mask byte lane select	Vdd2			
SDRADDR[10:0]	–	O	SDRAM address (Note 8)	Vdd2			
SDRBA[1:0]	–	O	SDRAM bank select	Vdd2			
SDRDATA[15:0]	–	B	SDRAM Data	Vdd2			
Sum					0	0	0
EXTERNAL MEMORY I/F							
NCS0	Neg	O	Chip select0	Vdd2		○	○
GPIO06	–	B	GPIO			○	○
EXTINT06	–	I	External Interrupt 0–bit6			○	○
NCS1	Neg	O	Chip select1	Vdd2		○	○
RXD0	–	I	UART Ch0 receive Data			○	○
GPIO10	–	B	GPIO			○	○
EXTINT10	–	I	External Interrupt 1–bit0	Vdd2		○	○
NRD	Neg	O	Read enable			○	○
GPIO17	–	B	GPIO			○	○
EXTINT17	–	I	External Interrupt 1–bit7	Vdd2		○	○
NWRENWRL	Neg	O	Write enable, write enable low			○	○
GPIO30	–	B	GPIO			○	○
EXTINT30	–	I	External Interrupt 3–bit0	Vdd2		○	○
NHBNWRH	–	O	High byte select, write enable high			○	○
TXD0	–	O	UART Ch0 transmit Data			○	○
GPIO31	–	B	GPIO			○	○
EXTINT31	–	I	External Interrupt 3–bit1			○	○

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Table 2. JTAG/SWD (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)		
					TA	XA,XC	XB,XD
Multiplexed Function							
EXTERNAL MEMORY I/F							
NLBEXA0	–	O	Low byte select, address0	Vdd2		○	○
GPIO16	–	B	GPIO			○	○
EXTINT16	–	I	External Interrupt 1–bit6			○	○
EXA[20:15]	–	O	Address	Vdd2			
GPIO4[5:0]	–	B	GPIO				
EXTINT4[5:0]	–	I	External Interrupt 4–bit5 to bit0				
EXA[14:9]	–	O	Address	Vdd2			
GPIO3[F:A]	–	B	GPIO				
EXTINT3[F:A]	–	I	External Interrupt 3–bit15 to bit10				
EXA[8:1]	–	O	Address	Vdd2			
GPIO3[9:2]	–	B	GPIO				
EXTINT3[9:2]	–	I	External Interrupt 3–bit9 to bit2				
EXD[7:0]	–	B	Data	Vdd2		○	○
GPIO4[D:6]	–	B	GPIO			○	○
EXTINT4[D:6]	–	I	External Interrupt 4–bit13 to bit6			○	○
EXD[15:8]	–	B	Data	Vdd2			
GPIO5[5:0] GPIO4[F:E]	–	B	GPIO				
EXTINT5[5:0] EXTINT4[F:E]	–	I	External Interrupt 5–bit5 to bit0, External Interrupt 4–bit15 to bit14				
Sum					0	14	14

Xtal, PLL

XIN1	–	I	XTAL input (XT1)	VddXT1	○	○	○
XOUT1	–	O	XTAL output (XT1)	VddXT1	○	○	○
VddXT1	–	P	XTAL power supply (XT1)	–	○	○	○
VssXT1	–	P	XTAL ground (XT1)	–	○	○	○
XTALINFO[1:0]	–	B	XTAL frequency input (Note 9) XTALINFO[1:0] = G “00”: 24 MHz G “01”: 12 MHz G “10”: 20 MHz G “11”: 48 MHz Used for determining clock frequency setting while internal ROM boot. Bonding internally for “TA” product	Vdd2	○	○	○
VCNT1	–	O	PLL1 VCO control	AvddPLL1	○	○	○
AvddPLL1	–	P	PLL1 analog power supply	–	○	○	○
AvssPLL1	–	P	PLL1 analog ground	–	○	○	○
VCNT2	–	O	PLL2 VCO control	AvddPLL2	○ (Note 10)	○	○
AvddPLL2	–	P	PLL2 analog power supply	–	○ (Note 10)	○	○
VCNT3	–	O	PLL3 VCO control	AvddPLL3	○ (Note 11)	○	○

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Table 2. JTAG/SWD (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)		
Multiplexed Function					TA	XA,XC	XB,XD
Xtal, PLL							
AvddPLL3	–	P	PLL3 analog power supply	–	○ (Note 11)	○	○
AvssPLL2	–	P	PLL2/3 analog ground (Note 12)	–	○	○	○
Sum					10	14	14
USB-PHY							
USBDP	–	B	USB D+	AVddUSBPHY2 or AVddUSBPHY1	○	○	○
USBDM	–	B	USB D–	AVddUSBPHY2 or AVddUSBPHY1	○	○	○
USBEXT12	–	O	USB–PHY reference resistor	AVddUSBPHY2	○	○	○
AvddUSBPHY1	–	P	USB–PHY 1.0V analog power supply	–	○ 2	○ 2	○ 2
DVddUSBPHY1	–	P	USB–PHY 1.0V digital power supply. Connected to AVddUSBPHY1 internally in case of no DVddUSBPHY1 port available	–	○	○	○
AvddUSBPHY2	–	P	USB–PHY 3.3V analog power supply	–	○ 2	○ 2	○ 2
AvddUSBPHY	–	P	USB–PHY analog ground	–	○ 4	○ 4	○ 4
Sum					11	11	11
10BIT ADC							
AN[5:0]	–	I	ADC Input	AVddADC	○	○	○
VRH	–	I	ADC High reference	AVddADC			
VRL	–	I	ADC Low reference	AVddADC			
VR	–	O	ADC reference voltage	AVddADC			
AVddADC	–	P	ADC analog power	–	○	○	○
AVssADC	–	P	ADC analog ground	–	○	○	○
Sum					8	8	8
CLASS-D AMP							
LOUT GPOUT	–	O O	Lch Class D AMP Output General purpose Output (GPO)	Avdd–DAMPL	○ ○	○	○ ○
ROUT GPROUT	–	O O	Rch Class D AMP Output General purpose Output (GPO)	Avdd–DAMPR	○ ○	○	○ ○
AVddDAMPL	–	P	Lch Class D AMP analog power supply	–	○	○	○
AVddDAMPR	–	P	Rch Class D AMP analog power supply	–	○	○	○
AVssDAMPL	–	P	Lch Class D AMP analog power supply	–	○	○	○
AVssDAMPR	–	P	Rch Class D AMP analog power supply	–	○	○	○
Sum					6	6	6

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Table 2. JTAG/SWD (continued)

Terminal Name	Polarity	Direction	Function	IO POWER	Available (○)		
					TA	XA,XC	XB,XD
Multiplexed Function							
OTHER, POWER							
BMODE[1:0]	–	B	Bootmodeselect	Vdd2	○	○	○
TEST	Pos	I	Test mode (normally connect to ground)	Vdd2	○	○	○
NRES	Neg	I	LSI reset Input	Vdd2	○	○	○
Vdd1	–	P	Digital core power	–	○ 7	○ 7	○ 7
Vdd2	–	P	Digital IO power	–	○ 8	○ 8	○ 8
VddSD0	–	P	Digital IO power (SDI/F Ch0)	–	○	○	○
VddSD1	–	P	Digital IO power (SD(MS)/F Ch1)	–	○	○	○
VddSD2	–	P	Digital IO power (SDI/F Ch2)	–	○	○	○
VddQSPI	–	P	Digital IO power (QSPI)	–	○ 12	○ 14	○ 14
Sum					35	37	37
All Sum					128	154	154

6. This function is not available
7. Set according to the General RTC mode or KeyInt RTC mode. Bonding internally for “TA” product as described on Page 7.
8. SDRAM address bit is 13bit including SDRADDR [12:11].
9. Set according to the frequency of XT1 (12/20/24/48 MHz).
Bonding internally for “TA” product as described on Page 5.
10. Audio clock is generated by one of PLL2 (1 V) or PLL3 (3 V).
One of PLL2 or PLL3 is available for “TA” and “RA” product. Please refer to Page 5 for more information.
Both of PLL2 and PLL3 are available for “XA”, “XB”, “XC” and “XD” products.
11. Audio clock is generated by one of PLL2 (1 V) or PLL3 (3 V).
One of PLL2 or PLL3 is available for “TA” and “RA” product. Please refer to Page 5 for more information.
Both of PLL2 and PLL3 are available for “XA”, “XB”, “XC” and “XD” products.
12. Analog ground is shared by PLL2 and PLL3.
13. Unused Input terminals and input state terminals of bidirectional should be set Pull-up/Down resistor ON or connect to digital power supply or ground (don't let open).

引导模式

根据BMODE[1:0]端口状态提供引导模式

Table 3. BOOT MODE

IPL Mode	BMODE1	BMODE0	Explanation
Physical Boot USB	PD 470 kΩ	PD 470 kΩ	Internal ROM boot(eMMC Physical Boot with USB download – SD card I/F Ch0 + USB Device + EXTINT2E + EXTINT2F)
			By using Boot operation mode of eMMC, load IPL2(program) from eMMC connected to SD0 to internal SRAM and jump to IPL2. IPL2 is written through USB.
Physical Boot SD	PD 470 kΩ	PU 470 kΩ	Internal ROM boot (eMMC Physical Boot with SD Ch1 download – SD card I/F Ch0 + SD card I/F Ch1 + EXTINT2E + EXTINT2F)
			By using Boot operation mode of eMMC, load IPL2(program) from eMMC connected to SD0 to internal SRAM and jump to IPL2. IPL2 is written through SD1.
User Area Boot USB	PD 1 kΩ	PU or PD 470 kΩ	Internal ROM boot(User Area Boot with USB download – SD card I/F Ch0 + USB Device + EXTINT2E + EXTINT2F)
			Load IPL2(program) from user area of eMMC connected to SD0 to internal SRAM and jump to IPL2. IPL2 is written through USB.
User Area Boot SD	PU 470 kΩ	PD 1 kΩ	Internal ROM boot(User Area Boot with SD Ch1 download – SD card I/F Ch0 + SD card I/F Ch1 + EXTINT2E + EXTINT2F)
			Load IPL2(program) from user area of eMMC connected to SD0 to internal SRAM and jump to IPL2. IPL2 is written through SD1.
SPI Boot USB	PU 470 kΩ	PU 470 kΩ	Internal ROM boot(external Serial Flash SPI Boot with USB down- load – S–Flash I/F + USB Device + EXTINT2E + EXTINT2F + TI- OCB01)
			Load IPL2(program) from Serial Flash connected to S–Flash I/F to internal SRAM and jump to IPL2. IPL2 is written through USB.
SPI Boot SD	PD 470 kΩ	PU 1 kΩ	Internal ROM boot(external Serial Flash SPI Boot with SD Ch1 download – S–Flash I/F + SD card I/F Ch1 + EXTINT2E + EXTINT2F + TIOCB01)
			Load IPL2 (program) from Serial Flash connected to S–Flash I/F to internal SRAM and jump to IPL2. IPL2 is written through SD1.
QSPI Boot USB	PU 1 kΩ	PU 470 kΩ	Internal ROM boot (external Serial Flash QSPI Boot with USB download – S–Flash I/F(QSPI) + USB Device + EXTINT2E + EXTINT2F + TIOCB01)
			Fetch IPL2 (program) from Serial Flash connected to S–Flash I/F. IPL2 is written by using DO command directly through USB.
QSPI Boot SD	PU 1 kΩ	PD 470 kΩ	Internal ROM boot (external Serial Flash QSPI Boot with SD Ch1 download – S–Flash I/F(QSPI) + SD card I/F Ch1 + EXTINT2E + EXTINT2F + TIOCB01)
			Fetch IPL2 (program) from Serial Flash connected to S–Flash I/F. IPL2 is written through SD1.
User Area Delete	PD 1 kΩ	PU 1 kΩ	Internal ROM boot (User Area IPL2 delete – SD card I/F Ch0 + EXTINT2E + EXTINT2F)
			After deleting IPL2 by using this mode, IPL2 can be written again while User Area Boot mode.

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Table 3. BOOT MODE (continued)

IPL Mode	BMODE1	BMODE0	Explanation
Partition Delete	PD 470 kΩ	PD 1 kΩ	Internal ROM boot (Partition Area IPL2 delete – SD card I/F Ch0 + EXTINT2E + EXTINT2F)
			After deleting IPL2 by using this mode, IPL2 can be written again while eMMC Physical Boot mode.
SPI All Erase	PU 470 kΩ	PU 1 kΩ	Internal ROM boot(external Serial Flash SPI all area delete – S–Flash I/F + EXTINT2E + EXTINT2F + TIOCB01)
			Delete all content of Serial Flash. This mode should be used in case of SPI mode operation of Serial Flash
SDCH0 All Erase	PD 1 kΩ	PD 1 kΩ	Internal ROM boot(all area delete – SD card I/F Ch0 + EXTINT2E + EXTINT2F)
			Delete all content of eMMC including Partition area. Take a lot of time to delete. Trim also processed in case of eMMC supporting Trim function.
QSPI All Erase	PU 1 kΩ	PD 1 kΩ	Internal ROM boot(external Serial Flash QSPI all area delete – S–Flash I/F(QSPI) + EXTINT2E + EXTINT2F + TIOCB01)
			Delete all content of Serial Flash. This mode should be used in case of QSPI fetch mode operation of Serial Flash
External ROM Boot	PU 470 kΩ	PD 470 kΩ	External memory boot(External–0)
			Fetch from external memory(External0) connected to XMC(external memory controller)
Hi–z	PU 1 kΩ	PU 1 kΩ	External I/F ports below forced to Hi–z – EXA[20:1], EXD[15:0], NCS[1:0], NRD, NWRENWRL, NHBNWRH, NLBEXA0 – SDCLK0, SDCMD0, SDAT0[3:0] – CK1, SD11(QIO0), SDO1(QIO1), SWP1(QIO2), SHOLD1(QIO3), TIOCB01

14. In case of TQFP128L, WLP154, don't use external memory boot (External–0)

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引导端口

在进行如下所示的引导时，某些端口将使用内部ROM代码。

- EXTINT2E(GPIO2E): OUT, 用于电源控制
- EXTINT2F(GPIO2F): OUT, 用于通过此端口的低/高信号指示引导状态、指示USB连接和USB中断连接的开始、错误状态。
- 将SDCMD1、SDAT1[3:0]、SDCLK1用作SD1。不使用SDCD1和SDWP1。从SD1写入时，处理端口功能切换。
- 使用4个端口(SCK1、QSCS、SDO1、SDI1)处理SPI Boot/SPI全部清除。不使用SHOLD1和SWP1。
- 使用SCK1、QSCS、SDO1、SDI1、SHOLD1、SWP1处理QSPI Boot/QSPI全部清除。
- 使用NCS0和外部存储控制器端口处理外部ROM引导。不使用GPIO2E。
- 如果外部I/F端口处于HiZ模式，则使用NCS0、NCS1和外部存储控制器等外部存储器接口。GPIO2E用作输入端口。

Table 4. PORTS USED DURING IPL

IPL Mode	Ports Used (Note 15)
Physical Boot USB	P2E(power supply control), P2F(status monitoring)
Physical Boot SD	P2E(power supply control), P2F(status monitoring) P22(SDCLK1) P23(SDCMD1) P24(SDDATA10) P25(SDDATA11) P26(SDDATA12) P27(SDDATA13)
User Area Boot USB	P2E(power supply control), P2F(status monitoring)
User Area Boot SD	P2E(power supply control), P2F(status monitoring) P22(SDCLK1) P23(SDCMD1) P24(SDDATA10) P25(SDDATA11) P26(SDDATA12) P27(SDDATA13)
SPI Boot USB	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1)
SPI Boot SD	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1) P22(SDCLK1) P23(SDCMD1) P24(SDDATA10) P25(SDDATA11) P26(SDDATA12) P27(SDDATA13)
QSPI Boot USB	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1) P011(SWP1) P12(SHOLD1) P22(SDCLK1) P23(SDCMD1) P24(SDDATA10) P25(SDDATA11) P26(SDDATA12) P27(SDDATA13)
User Area Delete	P2E(power supply control), P2F(status monitoring)
Partition Delete	P2E(power supply control), P2F(status monitoring)
SPI Erase	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SPIOUT) P0E(SDI1)
SDCH0 All Erase	P2E(power supply control), P2F(status monitoring)
QSPI All Erase	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1) P11(SWP1) P12(SHOLD1)
External ROM Boot	P06(NCS0) P17(NRD) P30(NWRENWRL) P31(NHBNWRH) P16(NLBEXA0) P32(EXA01) P33(EXA02) P34(EXA03) P35(EXA06) P36(EXA05) P37(EXA06) P38(EXA07) P39(EXA08) P3A(EXA09) P3B(EXA10) P3C(EXA11) P3D(EXA12) P3E(EXA13) P3F(EXA14) P40(EXA15) P41(EXA16) P42(EXA17) P43(EXA18) P44(EXA19) P45(EXA20) P46(EXD00) P47(EXD01) P48(EXD02) P49(EXD03) P4A(EXD04) P4B(EXD05) P4C(EXD06) P4D(EXD07) P4E(EXD08) P4F(EXD09) P50(EXD10) P51(EXD11) P52(EXD12) P53(EXD13) P54(EXD14) P55(EXD15)
HI-z	SDCLK0 Hi-z state

15. In this table "Pxx" means "GPIOxx". For example "P2E" means "GPIO2E".

SDIF上拉

在使用SDIF端口的引导模式中，将会使用上拉电阻 (SDCMD0、SDAT0[3:0] / SDCMD1、SDAT1[3:0])。因此，电路板上不需要使用外部上拉电阻。

QSCS上拉

在使用QSCS的引导模式中，通过硬复位启用GPIO03 (QSCS)上拉。在将GPIO2E设为“高”后，GPIO03将设为QSCS，且“上拉”设为停用。

如果是Hi-z引导模式，则“上拉”将被强制设为停用。

GPIO2F

在引导期间，GPIO2F将用作GPIO，通过低/高输出指示引导状态和错误情况。

在引导序列中，如果出现错误，例如IPL2写入错误，则GPIO2F将报告错误类型。GPIO0F可指示USB连接状态，以及USB文件传输的完成状态。可通过低/高序列报告删除模式、清除完成状态和清除状态。

关于引导期间所用端口行为的更多详情，请参阅文档“LC823450串行IPL规格”。

引脚分配

Table 5. PIN ASSIGNMENT

I/O		Input Type		Output Type	
I	Input	CMOS	CMOS Input	3-State	Tristate Output
O	Output	schmitt	schmitt Input	OD	Open Drain Output
B	Bidirectional	X	Xtal	X	Xtal
P	Power	3A	3.3 V analog	3A	3.3 V analog
NC	Non Connect	1A	1.0 V analog	1A	1.0/1.2 V analog

Drive (example)		PU/PD		IO Circuit Type	
4 mA	3.3 V 4 mA Output	PU	Pull-up resistor	Refer to Page 30 for circuit diagram	
4/8 mA	3.3 V with 4 mA, 8 mA output drivability switch	PD	Pull-down resistor		
0.3 mA-OD	1.0 V 0.3 mA open drain Output	PU/PD	Pull-up, pull-down resistor		

Table 6.

XBGA240		TQFP128L		WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No.	Ball									
1	R16	-	-		SDRDATA2	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)	
2	N14	1	1	M11	Vss	G							
3	P15	2	2	N12	Vdd2	P							
4	P16	3	3	H8	TCLKA0/ BCK1/ GPIO00/ EXTINT00	I/ B/ B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
5	N15	-	-		SDRDATA3	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)	
6	N16	4	4	L10	TCLKB0/ LRCK1/ GPIO01/ EXTINT01	I/ B/ B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
7	M16	-	5	K9	NHBNWRH/ TXD0/ GPIO31/ EXTINT31	O/ O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
8	M15	-	6	N11	NCS1/ RXD0/ GPIO10/ EXTINT10	O/ I/ B/ I	Schmitt	3-State	2/4/8 mA	PU	Vdd2	3ISU/3T2 (4)(8)	

Table 6.

XBGA240		TQFP128L		WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball									
9	M14	-	-		SDRDATA4	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)	
10	M13	-	7	M10	NCS0/ GPIO06/ EXTINT06	O/ B/ I	Schmitt	3-State	2/4/8 mA	PU	Vdd2	3ISU/3T2 (4)(8)	
11	L16	-	-		GPIO2A/ EXTINT2A/ SDRADDR12	B/ I/ O	Schmitt	3-State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T2 (4)(8)	
12	L15	-	-		Vdd2	P							
13	L14	-	-		Vss	G							
14	L13	5	8	L9	Vdd1	P							
15	L12	-	9	N10	NRD/ GPIO17/ EXTINT17	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
16	K16	-	-		SDRADDR5	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)	
17	K15	-	-		SDRADDR6	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)	
18	K14	-	10	M9	NWRENWRL/ GPIO30/ EXTINT30	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
19	K13	-	11	N9	EXD0/ GPIO46/ EXTINT46	B/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
20	K12	-	-		SDRADDR7	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)	
21	H13	-	-		SDRDATA5	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)	
22	J14	-	-		SDRDATA6	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)	
23	J13	-	-		Vdd2	P							
24	H10	-	-		Vss	G							
25	J12	-	-		SDRDATA7	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)	
26	J11	-	-		SDRDATA8	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)	
27	H11	-	-		SDRDATA9	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)	
28	H16	6	12	J8	SCK1/ GPIO0D/ EXTINT0D	O/ B/ I	Schmitt	3-State	6/8/10 mA	PU/PD	VddQSPI	3ISUD/3T6 (8)(10)	
29	H14	7	13	N8	TIOCB01/ DMCKO0/ QSCS/ GPIO03/ EXTINT03	B/ O/ O/ B/ I	Schmitt	3-State	6/8/10 mA	PU/PD	VddQSPI	3ISUD/3T6 (8)(10)	
30	J16	8	14	M8	SDO1(QIO1)/ GPIO0F/ EXTINT0F	I(B)/ B/ I	Schmitt	3-State	6/8/10 mA	PU/PD	VddQSPI	3ISUD/3T6 (8)(10)	
31	G14	9	15	L8	VddQSPI	P							
32	H15	10	16	K8	SD1(QIO0)/ GPIO0E/ EXTINT0E	O(B) / B/ I	Schmitt	3-State	6/8/10 mA	PU/PD	VddQSPI	3ISUD/3T6 (8)(10)	
33	J15	11	17	N7	Vss	G							
34	G16	12	18	M7	SWP1(QIO2)/ GPIO11/ EXTINT11	O(B) / B/ I	Schmitt	3-State	6/8/10 mA	PU/PD	VddQSPI	3ISUD/3T6 (8)(10)	
35	G15	13	19	L7	SHOLD1(QIO3)/ GPIO12/ EXTINT12	O(B) / B/ I	Schmitt	3-State	6/8/10 mA	PU/PD	VddQSPI	3ISUD/3T6 (8)(10)	
36	H12	14	20	K7	TXD2/ TIOCA10/ GPIO0B/ EXTINT0B	O/ B/ B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	VddQSPI	3ISUD/3T1 (2)(4)	

Table 6.

XBGA240		TQFP128L	WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball								
37	G13	15	21	J7	RXD2/ TIOCA11/ GPIO0C/ EXTINT0C	I/ B/ B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	VddQSPI	3ISUD/3T1 (2)(4)
38	G12	16	22	N6	TDI/ SDCD1/ SWO/ GPIO20/ EXTINT20	I/ I/ O/ B/ I	Schmitt	3-State	2 mA	PU/PD	VddSD1	3ISUD/3T2
39	G11	17	23	M6	TDO/ SDWP1/ INS/ GPIO21/ EXTINT21	O/ I/ I/ B/ I	Schmitt	3-State	2 mA	PU/PD	VddSD1	3ISUD/3T2
40	F16	18	24	L6	SDCMD1/ BS/ GPIO23/ EXTINT23	B/ O/ B/ I	CMOS	3-State	6/8/10 mA	PU/PD	VddSD1	3ICUD/3T6 (8)(10)
41	F15	19	25	K6	SDAT10/ DATA0/ GPIO24/ EXTINT24	B/ B/ B/ I	CMOS	3-State	6/8/10 mA	PU/PD	VddSD1	3ICUD/3T6 (8)(10)
42	F14	20	26	N5	VddSD1	P						
43	E14	21	27	M5	SDAT11/ DATA1/ GPIO25/ EXTINT25	B/ B/ B/ I	CMOS	3-State	6/8/10 mA	PU/PD	VddSD1	3ICUD/3T6 (8)(10)
44	F13	22	28	L5	Vss	G						
45	E16	23	29	J6	SDAT12/ DATA2/ GPIO26/ EXTINT26	B/ B/ B/ I	CMOS	3-State	6/8/10 mA	PU/PD	VddSD1	3ICUD/3T6 (8)(10)
46	E15	24	30	N4	SDAT13/ DATA3/ GPIO27/ EXTINT27	B/ B/ B/ I	CMOS	3-State	6/8/10 mA	PU/PD	VddSD1	3ICUD/3T6 (8)(10)
47	D16	25	31	M4	SDCLK1/ SCLK/ GPIO22/ EXTINT22	O/ O/ B/ I	CMOS	3-State	6/8/10 mA	PU/PD	VddSD1	3ICUD/3T6 (8)(10)
48	F12	-	-		SDRADDR8	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)
49	E12	-	-		SDRADDR9	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)
50	F11	-	-		SDRADDR10	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)
51	E13	26	32	L4	Vdd1	P						
52	D13	27	33	N3	Vss	G						
53	D14	28	34	N2	Vdd2	P						
54	D15	-	-		SDRBA0	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)
55	C16	-	-		SDRBA1	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)
56	C15	-	-		SDRCAS	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)
57	C14	-	-		SDRRAS	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)
58	B16	-	-		Vdd2	P						
59	B15	-	-		Vss	G						
60	A16	-	-		SDRCKE	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)
61	A15	-	-		SDRCLK	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)
62	A14	29	35	M3	SDCLK0	O	CMOS	3-State	6/8/10 mA		VddSD0	3IC/3T6 (8)(10)
63	B14	30	36	K5	SDCMD0	B	CMOS	3-State	6/8/10 mA	PU/PD	VddSD0	3ICUD/3T6 (8)(10)
64	C12	31	37	N1	VddSD0	P						
65	B13	32	38	L3	SDAT00	B	CMOS	3-State	6/8/10 mA	PU/PD	VddSD0	3ICUD/3T6 (8)(10)
66	C13	33	39	M2	Vss	G						

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Table 6.

XBGA240		TQFP128L	WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball								
67	A13	34	40	K4	SDAT01	B	CMOS	3-State	6/8/10 mA	PU/PD	VddSD0	3ICUD/3T6 (8)(10)
68	A12	35	41	M1	SDAT02	B	CMOS	3-State	6/8/10 mA	PU/PD	VddSD0	3ICUD/3T6 (8)(10)
69	B12	36	42	J5	SDAT03	B	CMOS	3-State	6/8/10 mA	PU/PD	VddSD0	3ICUD/3T6 (8)(10)
70	C11	37	43	K3	TIOCA01/ SDCMD2/ PHI1/ GPIO0A/ EXTINT0A	B/ B/ O/ B/ I	CMOS	3-State	6/8/10 mA	PU/PD	VddSD2	3ICUD/3T6 (8)(10)
71	A11	38	44	L2	TXD1/ SDAT20/ GPIO04/ EXTINT04	O/ B/ B/ I	CMOS	3-State	6/8/10 mA	PU/PD	VddSD2	3ICUD/3T6 (8)(10)
72	B11	39	45	J4	RXD1/ SDAT21/ GPIO05/ EXTINT05	I/ B/ B/ I	CMOS	3-State	6/8/10 mA	PU/PD	VddSD2	3ICUD/3T6 (8)(10)
73	D12	40	46	L1	VddSD2	P						
74	C10	41	47	H6	CTS1/ SDAT22/ RXD0/ GPIO56/ EXTINT56	I/ B/ I/ B/ I	CMOS	3-State	6/8/10 mA	PU/PD	VddSD2	3ICUD/3T6 (8)(10)
75	E11	42	48	K2	Vss	G						
76	B10	43	49	K1	RTS1/ SDAT23/ TXD0/ GPIO57/ EXTINT57	O/ B/ O/ B/ I	CMOS	3-State	6/8/10 mA	PU/PD	VddSD2	3ICUD/3T6 (8)(10)
77	D11	44	50	J3	TCK/ SDCD2/ GPIO29/ EXTINT29	I/ I/ B/ I	Schmitt	3-State	1/2/4mA	PU/PD	VddSD2	3ISUD/3T1 (2)(4)
78	D10	45	51	H5	TMS/ SDWP2/ GPIO28/ EXTINT28	I/ I/ B/ I	Schmitt	3-State	1/2/4mA	PU/PD	VddSD2	3ISUD/3T1 (2)(4)
79	A10	46	52	J2	TIOCA00/ SDCLK2/ PHI0/ GPIO09/ EXTINT09	B/ O/ O/ B/ I	Schmitt	3-State	6/8/10 mA	PU/PD	VddSD2	3ISUD/3T6 (8)(10)
80	E10	-	-		SDRCS	O	-	3-State	2/4/8mA		Vdd2	3T2 (4)(8)
81	F10	-	-		SDRWE	O	-	3-State	2/4/8mA		Vdd2	3T2 (4)(8)
82	G10	-	-		SDRDQM0	O	-	3-State	2/4/8mA		Vdd2	3T2 (4)(8)
83	D9	-	-		SDRDQM1	O	-	3-State	2/4/8mA		Vdd2	3T2 (4)(8)
84	E9	-	-		SDRDATA10	B	CMOS	3-State	2/4/8mA	PD	Vdd2	3ICD/3T2 (4)(8)
85	F9	-	-		SDRDATA11	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
86	A9	47	53	J1	Vdd1	P						
87	B9	48	54	H4	Vss	G						
88	G9	-	55	G5	XTALINFO0	B	Schmitt	3-State	2/4/8 mA	PU	Vdd2	3ISU/3T2 (4)(8)
89	C9	49	56	H1	Vdd2	P						
90	H9	-	-		SDRDATA12	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
91	G8	-	-		SDRDATA13	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
92	F8	-	-		SDRDATA14	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
93	E8	-	-		SDRDATA15	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)

Table 6.

XBGA240		TQFP128L	WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball								
94	D8	50	57	H2	VddRTC	P						
95	A7	–	58	H3	RTCMODE	I	CMOS	–	–	–	VddRTC	1IC
96	B8	51	59	G2	VssRTC	G						
97	A8	52	60	G1	XIN32K	I	X	–	–	–	VddRTC	X
98	C8	53	61	G3	XOUT32K	O	–	X	–	–	VddRTC	X
99	B7	54	62	F1	VDET	I	CMOS	–	–	–	VddRTC	1IC
100	C7	55	63	G4	RTCINT(Note 16)	O	–	OD	0.3 mA–OD	–	VddRTC	OD3
101	D7	56	64	F2	BACKUPB	I	Schmitt	–	–	–	VddRTC	1IS
102	E7	–	65	F3	KEYINT0	I	Schmitt	–	–	PD	VddRTC	1ISD
103	F7	–	66	F4	KEYINT1	I	Schmitt	–	–	PD	VddRTC	1ISD
104	G7	–	67	E1	KEYINT2	I	Schmitt	–	–	PD	VddRTC	1ISD
105	A6	57	68	E2	AVddADC	P						
106	B6	–	–		VRH	I	3A	–	–	–	AVddADC	3A
107	C6	–	–		VR	O	–	3A	–	–	AVddADC	3A
108	D6	–	–		VRL	I	3A	–	–	–	AVddADC	3A
109	E6	58	69	D1	AVssADC	G						
110	C5	59	70	E3	AN5	I	3A	–	–	–	AVddADC	3A
111	B5	60	71	D2	AN4	I	3A	–	–	–	AVddADC	3A
112	A5	61	72	D3	AN3	I	3A	–	–	–	AVddADC	3A
113	C4	62	73	C1	AN2	I	3A	–	–	–	AVddADC	3A
114	B4	63	74	C2	AN1	I	3A	–	–	–	AVddADC	3A
115	A4	64	75	B1	AN0	I	3A	–	–	–	AVddADC	3A
116	D5	–	76	F5	NLBEXA0/ GPIO16/ EXTINT16	O/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
117	F6	–	77	E4	EXD1/ GPIO47/ EXTINT47	B/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
118	A3	–	–		EXA1/ GPIO32/ EXTINT32	O/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
119	B3	–	–		EXA2/ GPIO33/ EXTINT33	O/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
120	A2	–	–		EXA3/ GPIO34/ EXTINT34	O/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
121	A1	–	–		Vss	G						
122	B2	–	–		Vdd2	P						
123	B1	–	–		EXA4/ GPIO35/ EXTINT35	O/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
124	C1	–	–		EXA5/ GPIO36/ EXTINT36	O/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
125	C2	–	–		EXA6/ GPIO37/ EXTINT37	O/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
126	C3	65	78	A1	SCL0/ GPIO07/ EXTINT07	O/ B/ I	Schmitt	3–State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
127	D3	–	–		EXA7/ GPIO38/ EXTINT38	O/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
128	D4	66	79	B2	SDA0/ GPIO08/ EXTINT08	B/ B/ I	Schmitt	3–State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)

Table 6.

XBGA240		TQFP128L		WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball									
129	E4	-	-		EXA8/ GPIO39/ EXTINT39	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
130	E5	67	80	C3	SDO0/ GPIO1F/ EXTINT1F	O/ B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
131	D1	68	81	D4	Vss	G							
132	D2	69	82	A2	Vdd2	P							
133	F4	-	-		EXA9/ GPIO3A/ EXTINT3A	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
134	F5	-	-		EXA10/ GPIO3B/ EXTINT3B	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
135	G5	-	-		EXA11/ GPIO3C/ EXTINT3C	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
136	G4	70	83	B3	SCK0/ GPIO1D/ EXTINT1D	B/ B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
137	G6	-	-		EXA12/ GPIO3D/ EXTINT3D	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
138	H4	71	84	A3	SWDCLK/ GPIO58/ EXTINT58/ DMCKO1	I/ B/ I/ O	Schmitt	3-State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
139	H5	-	-		EXA13/ GPIO3E/ EXTINT3E	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
140	H6	72	85	F6	SDIO/ GPIO1E/ EXTINT1E	I/ B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
141	J4	-	-		EXA14/ GPIO3F/ EXTINT3F	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
142	J5	73	86	C4	SWDIO/ GPIO59/ EXTINT59/ DMDIN1	B/ B/ I/ I	Schmitt	3-State	2 mA	PU	Vdd2	3ISU/3T2	
143	H7	-	87	E5	EXD2/ GPIO48/ EXTINT48	B/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
144	J6	-	88	A4	EXD3/ GPIO49/ EXTINT49	B/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
145	E3	74	89	B4	Vdd1	P							
146	F3	-	-		Vdd2	P							
147	G3	-	90	D5	Vss	G							
148	K6	-	-		EXA15/ GPIO40/ EXTINT40	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
149	K5	-	-		EXA16/ GPIO41/ EXTINT41	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
150	L5	-	-		EXA17/ GPIO42/ EXTINT42	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
151	M4	-	-		EXA18/ GPIO43/ EXTINT43	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
152	K4	-	-		Vss	G							
153	E2	-	-		DVddUSBPHY1	P							
154	F2	75	91	A5	AVddUSBPHY1	P							
155	G2	76	92	C5	AVssUSBPHY	G							

Table 6.

XBGA240		TQFP128L	WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball								
156	E1	77	93	B5	USBDM	B	3A	3A	-	-	AVddUSB PHY2	3A
157	F1	78	94	B6	USBDP	B	3A	3A	-	-	AVddUSB PHY2	3A
158	G1	79	95	C6	AVssUSBPHY	G						
159	H2	80	96	D6	AVddUSBPHY2	P						
160	J1	81	97	E6	AVssUSBPHY	G						
161	H1	82	98	B7	USBEXT12	O	-	3A	-	-	AVddUSB PHY2	3A
162	J2	83	99	C7	AVddUSBPHY2	P						
163	H3	84	100	D7	AVddUSBPHY1	P						
164	J3	85	101	E7	AVssUSBPHY	G						
165	K3	-	-		DVddUSBPHY1	P						
166	L1	-	-		Vss	G						
167	K2	86	102	B8	VddXT1	P						
168	K1	87	103	A8	XIN1	I	X	-	-	-	VddXT1	X
169	L2	88	104	D8	VssXT1	G						
170	L3	89	105	C8	XOUT1	O	-	X	-	-	VddXT1	X
171	L4	90	106	E8	Vdd1	P						
172	M3	-	-		Vss	G						
173	M2	91	107	A9	AVddPLL1	P						
174	M1	92	108	B9	VCNT1	O	-	1A	-	-	AVddPLL1	1A
175	N1	93	109	C9	AVssPLL1	G						
176	N3	-	110	A10	EXD4/ GPIO4A/ EXTINT4A	B/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
177	N2	-	-		Vss	G						
178	P1	-	-		Vdd2	P						
179	P2	-	111	B10	EXD5/ GPIO4B/ EXTINT4B	B/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
180	R1	-	112	D9	EXD6/ GPIO4C/ EXTINT4C	B/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
181	R2	-	-		EXA19/ GPIO44/ EXTINT44	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
182	R3	-	-		EXA20/ GPIO45/ EXTINT45	O/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
183	P3	-	113	A11	EXD7/ GPIO4D/ EXTINT4D	B/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
184	N4	94	114	F7	TIOCB00/ DMDIN0/ DIN1/ GPIO02/ EXTINT02	B/ I/ I/ B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
185	R4	-	115	B11	Vss	G						
186	P4	95	116	A12	Vdd2	P						
187	M6	96	117	C10	DOU1/ GPIO15/ EXTINT15	O/ B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
188	N5	-	-		EXD8/ GPIO4E/ EXTINT4E	B/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)
189	M5	-	-		EXD9/ GPIO4F/ EXTINT4F	B/ B/ I	Schmitt	3-State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)

Table 6.

XBGA240		TQFP128L		WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball									
190	L6	–	118	G6	BCK1/ GPIO13/ EXTINT13	B/ B/ I	Schmitt	3–State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
191	M7	–	–		EXD10/ GPIO50/ EXTINT50	B/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
192	N7	–	119	G7	LRCK1/ GPIO14/ EXTINT14	B/ B/ I	Schmitt	3–State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
193	N6	97	120	B12	MCLK0/ MCLK1/ GPIO18/ EXTINT18	B/ B/ B/ I	Schmitt	3–State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
194	L7	–	–		EXD11/ GPIO51/ EXTINT51	B/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
195	M8	98	121	H7	BCK0/ DMCKO1/ GPIO19/ EXTINT19	B/ O/ B/ I	Schmitt	3–State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
196	K7	–	–		EXD12/ GPIO52/ EXTINT52	B/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
197	P5	99	122	C11	Vdd2	P							
198	J7	–	123	D10	XTALINFO1	B	Schmitt	3–State	2/4/8 mA	PU	Vdd2	3ISU/3T2 (4)(8)	
199	P6	100	124	C12	Vss	G							
200	L8	–	–		EXD13/ GPIO53/ EXTINT53	B/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
201	K8	101	125	E9	LRCK0/ DMDIN1/ GPIO1A/ EXTINT1A	B/ I/ B/ I	Schmitt	3–State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
202	J8	–	–		EXD14/ GPIO54/ EXTINT54	B/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
203	N9	102	126	F8	DINO/ DMDINO/ GPIO1B/ EXTINT1B	I/ I/ B/ I	Schmitt	3–State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
204	M9	–	–		EXD15/ GPIO55/ EXTINT55	B/ B/ I	Schmitt	3–State	2/4/8 mA	PD	Vdd2	3ISD/3T2 (4)(8)	
205	N8	103	127	E10	DOU0/ DMCKO0/ GPIO1C/ EXTINT1C	O/ O/ B/ I	Schmitt	3–State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)	
206	P7	104	128	D11	NRES	I	Schmitt	–	–	–	Vdd2	3IS	
207	L9	105	129	D12	BMODE0	B	Schmitt	3–State	2 mA	PU/PD	Vdd2	3ISUD/3T2	
208	K9	106	130	F9	BMODE1	B	Schmitt	3–State	2 mA	PU/PD	Vdd2	3ISUD/3T2	
209	J9	107	131	F10	TEST	I	Schmitt	–	–		Vdd2	3IS	
210	P8	108	132	E11	Vdd2	P							
211	H8	109	133	E12	Vss	G							
212	P9	110	134	G10	Vdd1	P							
213	R5	111	135	F11	AVssDAMPR	G							
214	R6	112	136	F12	ROUT/ GPROUT	O/ O	–	1A	–	–	AVddDAMPR	1A	
215	R7	113	137	G11	AVddDAMPR	P							
216	R8	114	138	G12	AVddDAMPL	P							
217	R9	115	139	H12	LOUT/ GPLOUT	O/ O	–	1A	–	–	AVddDAMPL	1A	
218	R10	116	140	H11	AVssDAMPL	G							

Table 6.

XBGA240		TQFP128L		WLP154		Pin Name	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball									
219	P10	-	-			Vdd1	P						
220	N11	117	141	H10		Vss	G						
(Note 18)		(Note 17)											
			142	J12		AVddPLL3	P						
			143	J11		VCNT3	O	-	3A	-	-	AVddPLL3	3A
221	P12	118	144	J10		AVssPLL2	G						
222	R12	119	145	K11		VCNT2	O	-	1A	-	-	AVddPLL2	1A
223	R13	120	146	K12		AVddPLL2	P						
224	P11	121	147	G9		Vdd1	P						
225	R11	-	-			Vss	G						
226	N12	-	-			Vdd2	P						
227	M10	122	148	H9		GPIO2D/ EXTINT2D/ DMCKO0/ SDRADDR11	B/ I/ O/ O	Schmitt	3-State	2/4/8 mA	PU/PD	Vdd2	3ISUD/3T (4)(8)
228	L10	-	-			SDRADDR0	O	-	3-State	2/4/8 mA		Vdd2	3T2(4)(8)
229	K10	123	149	G8		GPIO2E/ EXTINT2E	B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
230	J10	-	-			SDRADDR1	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)
231	N10	-	-			SDRADDR2	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)
232	M11	124	150	L12		GPIO2F/ EXTINT2F	B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
233	P13	125	151	L11		Vss	G						
234	L11	126	152	K10		SCL1/ GPIO2B/ EXTINT2B	O/ B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
235	R14	127	153	M12		Vdd2	P						
236	K11	128	154	J9		SDA1/ GPIO2C/ EXTINT2C	B/ B/ I	Schmitt	3-State	1/2/4 mA	PU/PD	Vdd2	3ISUD/3T1 (2)(4)
237	M12	-	-			SDRDATA0	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
238	N13	-	-			SDRDATA1	B	CMOS	3-State	2/4/8 mA	PD	Vdd2	3ICD/3T2 (4)(8)
239	P14	-	-			SDRADDR3	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)
240	R15	-	-			SDRADDR4	O	-	3-State	2/4/8 mA		Vdd2	3T2 (4)(8)

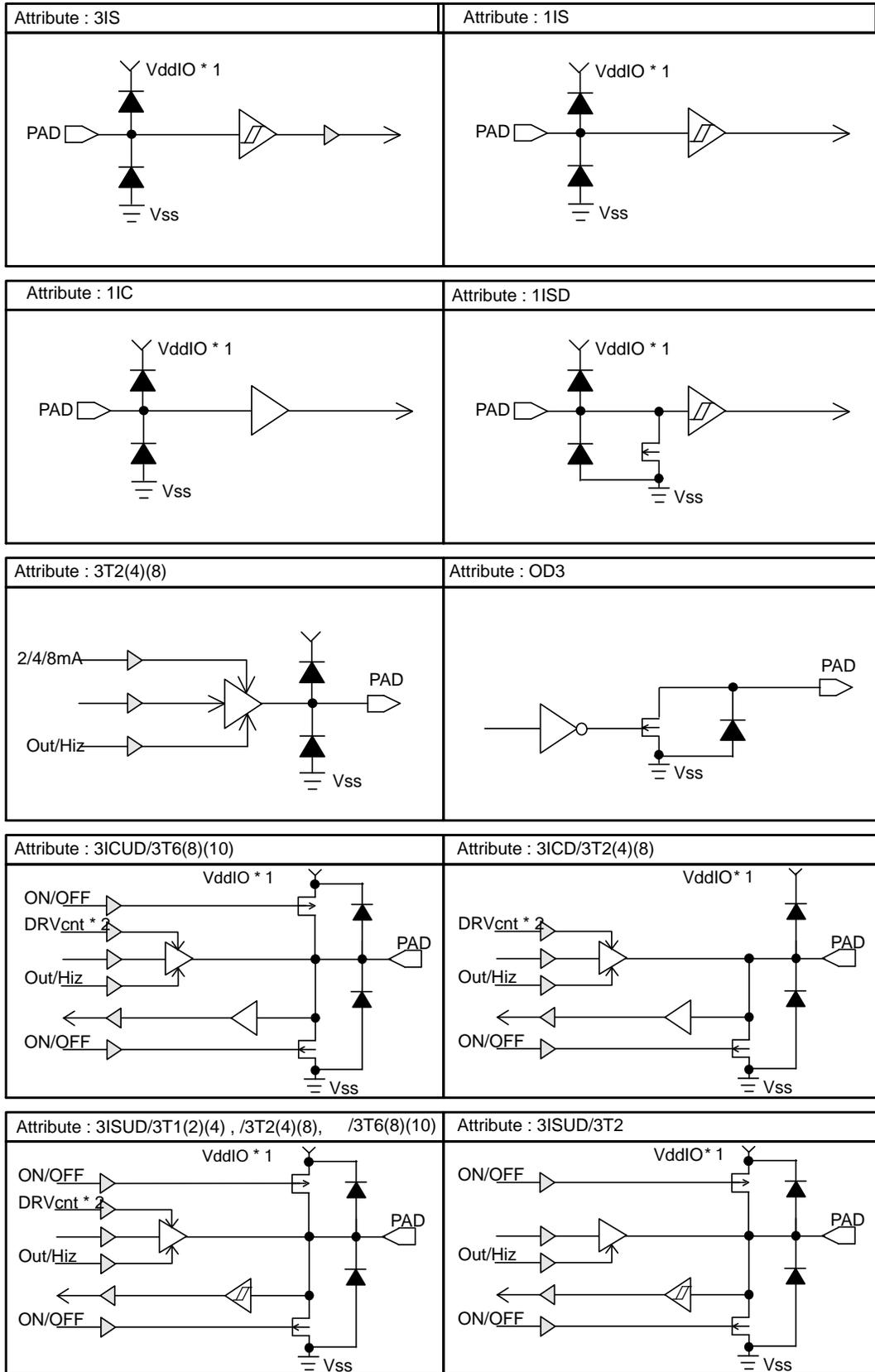
16. RTCINT (open drain Output) 3.6 V tolerant

17. Pin assignment for PLL3 of package TQFP128L is as below

PLL3	
118	AvddPLL3
119	VCNT3
120	AVssPLL2

18. PLL3 is unusable in package XBGA240.

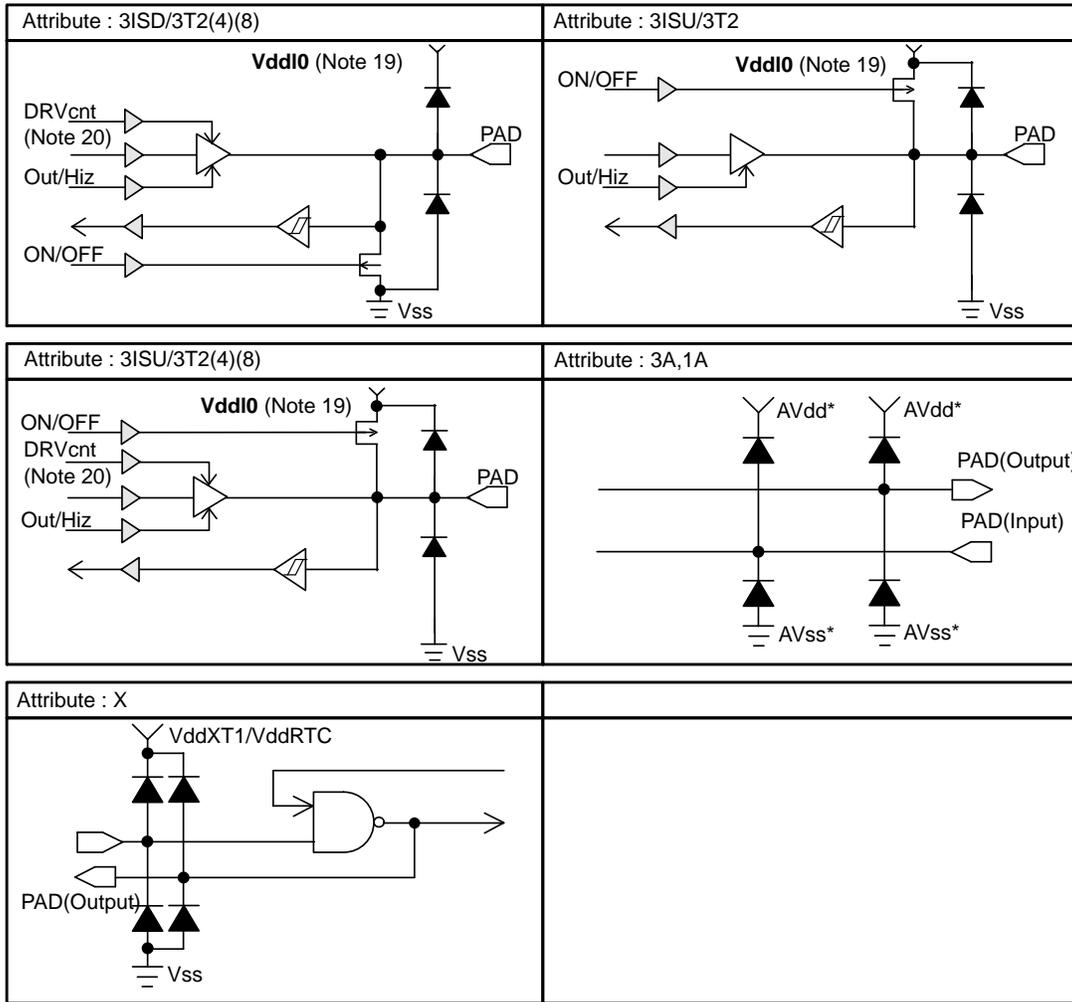
输入/输出电路



▷ Level Shifter

Figure 4. Input/Output Circuit

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▷ Level Shifter

19. Vdd2, VddSD0, VddSD1, VddSD2, VddQSPI (IO Pwr Grp of 3-1 Pin Assignment)
 20. DRVcnt: 1/2/4 mA, 2/4/8 mA, 4/8/10 mA, etc. Drivability switch control signal

Figure 5. Input/Output Circuit (Continued)

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Table 7. PORT STATE TABLE

XBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•	•	•	TCLKA0/ BCK1/ GPIO00/ EXTINT00	GPIO00	Hiz	Hiz
•	•	•	TCLKB0/ LRCK1/ GPIO01/ EXTINT01	GPIO01	Hiz	Hiz
•	•	•	TIOCB00/ DMDIN0 DIN1/ GPIO02/ EXTINT02/	GPIO02	Hiz	Hiz
•	•	•	TIOCB01/ DMCKO0/ QSCS/ GPIO03/ EXTINT03	GPIO03	PU	PU (Note 24)
•	•	•	TXD1/ SDAT20/ GPIO04/ EXTINT04	GPIO04	Hiz	Hiz
•	•	•	RXD1/ SDAT21/ GPIO05/ EXTINT05	GPIO05	Hiz	Hiz
•	•	•	NCS0/ GPIO06/ EXTINT06	GPIO06	Hiz	Hiz
•	•	•	SCL0/ GPIO07/ EXTINT07	GPIO07	Hiz	Hiz
•	•	•	SDA0/ GPIO08/ EXTINT08	GPIO08	Hiz	Hiz
•	•	•	TIOCA00/ SDCLK2/ PHI0/ GPIO09/ EXTINT09	GPIO09	Hiz	Hiz
•	•	•	TIOCA01/ SDCMD2/ PHI1/ GPIO0A/ EXTINT0A	GPIO0A	Hiz	Hiz
•	•	•	TXD2/ TIOCA10/ GPIO0B/ EXTINT0B	GPIO0B	Hiz	Hiz
•	•	•	RXD2/ TIOCA11/ GPIO0C/ EXTINT0C	GPIO0C	Hiz	Hiz
•	•	•	SCK1/ GPIO0D/ EXTINT0D	GPIO0D	Hiz	Hiz

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Table 7. PORT STATE TABLE (continued)

XBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•	•	•	SDI1(QIO0)/ GPIO0E/ EXTINT0E	GPIO0E	Hiz	Hiz
•	•	•	SDO1(QIO1)/ GPIO0F/ EXTINT0F	GPIO0F	Hiz	Hiz
•		•	NCS1/ RXD0/ GPIO10/ EXTINT10	GPIO10	Hiz	Hiz
•	•	•	SWP1(QIO2)/ GPIO11/ EXTINT11	GPIO11	Hiz	Hiz
•	•	•	SHOLD1(QIO3)/ GPIO12/ EXTINT12	GPIO12	Hiz	Hiz
•		•	BCK1/ GPIO13/ EXTINT13	GPIO13	Hiz	Hiz
•		•	LRCK1/ GPIO14/ EXTINT14	GPIO14	Hiz	Hiz
•	•	•	DOUT1/ GPIO15/ EXTINT15	GPIO15	Hiz	Hiz
•		•	NLBEXA0/ GPIO16/ EXTINT16	GPIO16	Hiz	Hiz
•		•	NRD/ GPIO17/ EXTINT17	GPIO17	Hiz	Hiz
•	•	•	MCLK0/ MCLK1/ GPIO18/ EXTINT18	GPIO18	Hiz	Hiz
•	•	•	BCK0/ DMCKO1/ GPIO19/ EXTINT19	GPIO19	Hiz	Hiz
•	•	•	LRCK0/ DMDIN1/ GPIO1A/ EXTINT1A	GPIO1A	Hiz	Hiz
•	•	•	DIN0/ DMDIN0/ GPIO1B/ EXTINT1B	GPIO1B	Hiz	Hiz
•	•	•	DOUT0/ DMCKO0/ GPIO1C/ EXTINT1C	GPIO1C	Hiz	Hiz
•	•	•	SCK0/ GPIO1D/ EXTINT1D	GPIO1D	Hiz	Hiz
•	•	•	SDI0/ GPIO1E/ EXTINT1E	GPIO1E	Hiz	Hiz

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Table 7. PORT STATE TABLE (continued)

XBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•	•	•	SDO0/ GPIO1F/ EXTINT1F	GPIO1F	Hiz	Hiz
•	•	•	TDI/ SDCD1/ SWO/ GPIO20/ EXTINT20	GPIO20	Hiz	Hiz
•	•	•	TDO/ SDWP1/ INS/ GPIO21/ EXTINT21	GPIO21	Hiz	Hiz
•	•	•	SDCLK1/ SCLK/ GPIO22/ EXTINT22	GPIO22	Hiz	Hiz
•	•	•	SDCMD1/ BS/ GPIO23/ EXTINT23	GPIO23	Hiz	Hiz
•	•	•	SDAT10/ DATA0/ GPIO24/ EXTINT24	GPIO24	Hiz	Hiz
•	•	•	SDAT11/ DATA1/ GPIO25/ EXTINT25	GPIO25	Hiz	Hiz
•	•	•	SDAT12/ DATA2/ GPIO26/ EXTINT26	GPIO26	Hiz	Hiz
•	•	•	SDAT13/ DATA3/ GPIO27/ EXTINT27	GPIO27	Hiz	Hiz
•	•	•	TMS/ SDWP2/ GPIO28/ EXTINT28	GPIO28	Hiz	Hiz
•	•	•	TCK/ SDCD2/ GPIO29/ EXTINT29	GPIO29	Hiz	Hiz
•			GPIO2A/ EXTINT2A/ SDRADDR12	GPIO2A	Hiz	Hiz
•	•	•	SCL1/ GPIO2B/ EXTINT2B	GPIO2B	Hiz	Hiz
•	•	•	SDA1/ GPIO2C/ EXTINT2C	GPIO2C	Hiz	Hiz
•	•	•	GPIO2D/ EXTINT2D/ DMCKO0/ SDRADDR11	GPIO2D	Hiz	Hiz

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Table 7. PORT STATE TABLE (continued)

XBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•	•	•	GPIO2E/ EXTINT2E	GPIO2E	Hiz	Hiz(Note 25)
•	•	•	GPIO2F/ EXTINT2F	GPIO2F	Hiz	Hiz(Note 26)
•		•	NWRENWRL/ GPIO30/ EXTINT30	GPIO30	Hiz	Hiz
•		•	NHBNWRH/ TXD0/ GPIO31/ EXTINT31	GPIO31	Hiz	Hiz
•			EXA1/ GPIO32/ EXTINT32	GPIO32	Hiz	Hiz
•			EXA2/ GPIO33/ EXTINT33	GPIO33	Hiz	Hiz
•			EXA3/ GPIO34/ EXTINT34	GPIO34	Hiz	Hiz
•			EXA4/ GPIO35/ EXTINT35	GPIO35	Hiz	Hiz
•			EXA5/ GPIO36/ EXTINT36	GPIO36	Hiz	Hiz
•			EXA6/ GPIO37/ EXTINT37	GPIO37	Hiz	Hiz
•			EXA7/ GPIO38/ EXTINT38	GPIO38	Hiz	Hiz
•			EXA8/ GPIO39/ EXTINT39	GPIO39	Hiz	Hiz
•			EXA9/ GPIO3A/ EXTINT3A	GPIO3A	Hiz	Hiz
•			EXA10/ GPIO3B/ EXTINT3B	GPIO3B	Hiz	Hiz
•			EXA11/ GPIO3C/ EXTINT3C	GPIO3C	Hiz	Hiz
•			EXA12/ GPIO3D/ EXTINT3D	GPIO3D	Hiz	Hiz
•			EXA13/ GPIO3E/ EXTINT3E	GPIO3E	Hiz	Hiz
•			EXA14/ GPIO3F/ EXTINT3F	GPIO3F	Hiz	Hiz

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Table 7. PORT STATE TABLE (continued)

XBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•			EXA15/ GPIO40/ EXTINT40	GPIO40	Hiz	Hiz
•			EXA16/ GPIO41/ EXTINT41	GPIO41	Hiz	Hiz
•			EXA17/ GPIO42/ EXTINT42	GPIO42	Hiz	Hiz
•			EXA18/ GPIO43/ EXTINT43	GPIO43	Hiz	Hiz
•			EXA19/ GPIO44/ EXTINT44	GPIO44	Hiz	Hiz
•			EXA20/ GPIO45/ EXTINT45	GPIO45	Hiz	Hiz
•		•	EXD0/ GPIO46/ EXTINT46	GPIO46	Hiz	Hiz
•		•	EXD1/ GPIO47/ EXTINT47	GPIO47	Hiz	Hiz
•		•	EXD2/ GPIO48/ EXTINT48	GPIO48	Hiz	Hiz
•		•	EXD3/ GPIO49/ EXTINT49	GPIO49	Hiz	Hiz
•		•	EXD4/ GPIO4A/ EXTINT4A	GPIO4A	Hiz	Hiz
•		•	EXD5/ GPIO4B/ EXTINT4B	GPIO4B	Hiz	Hiz
•		•	EXD6/ GPIO4C/ EXTINT4C	GPIO4C	Hiz	Hiz
•		•	EXD7/ GPIO4D/ EXTINT4D	GPIO4D	Hiz	Hiz
•			EXD8/ GPIO4E/ EXTINT4E	GPIO4E	Hiz	Hiz
•			EXD9/ GPIO4F/ EXTINT4F	GPIO4F	Hiz	Hiz
•			EXD10/ GPIO50/ EXTINT50	GPIO50	Hiz	Hiz
•			EXD11/ GPIO51/ EXTINT51	GPIO51	Hiz	Hiz

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Table 7. PORT STATE TABLE (continued)

XBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•			EXD12/ GPIO52/ EXTINT52	GPIO52	Hiz	Hiz
•			EXD13/ GPIO53/ EXTINT53	GPIO53	Hiz	Hiz
•			EXD14/ GPIO54/ EXTINT54	GPIO54	Hiz	Hiz
•			EXD15/ GPIO55/ EXTINT55	GPIO55	Hiz	Hiz
•	•	•	CTS1/ SDAT22/ RXD0/ GPIO56/ EXTINT56	GPIO56	Hiz	Hiz
•	•	•	RTS1/ SDAT23/ TXD0/ GPIO57/ EXTINT57	GPIO57	Hiz	Hiz
•	•	•	SDAT00	SDAT00	Hiz	Hiz
•	•	•	SDAT01	SDAT01	Hiz	Hiz
•	•	•	SDAT02	SDAT02	Hiz	Hiz
•	•	•	SDAT03	SDAT03	Hiz	Hiz
•	•	•	SDCLK0	SDCLK0	Low	Low
•	•	•	SDCMD0	SDCMD0	Hiz	Hiz
•			SDRADDR0	SDRADDR0	Low	Low
•			SDRADDR1	SDRADDR1	Low	Low
•			SDRADDR10	SDRADDR10	Low	Low
•			SDRADDR2	SDRADDR2	Low	Low
•			SDRADDR3	SDRADDR3	Low	Low
•			SDRADDR4	SDRADDR4	Low	Low
•			SDRADDR5	SDRADDR5	Low	Low
•			SDRADDR6	SDRADDR6	Low	Low
•			SDRADDR7	SDRADDR7	Low	Low
•			SDRADDR8	SDRADDR8	Low	Low
•			SDRADDR9	SDRADDR9	Low	Low
•			SDRBA0	SDRBA0	Low	Low
•			SDRBA1	SDRBA1	Low	Low
•			SDRCAS	SDRCAS	High	High
•			SDRCKE	SDRCKE	High	High
•			SDRCLK	SDRCLK	Low	Low
•			SDRCS	SDRCS	High	High
•			SDRDATA0	SDRDATA0	Hiz	Hiz
•			SDRDATA1	SDRDATA1	Hiz	Hiz

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Table 7. PORT STATE TABLE (continued)

XBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•			SDRDATA10	SDRDATA10	Hiz	Hiz
•			SDRDATA11	SDRDATA11	Hiz	Hiz
•			SDRDATA12	SDRDATA12	Hiz	Hiz
•			SDRDATA13	SDRDATA13	Hiz	Hiz
•			SDRDATA14	SDRDATA14	Hiz	Hiz
•			SDRDATA15	SDRDATA15	Hiz	Hiz
•			SDRDATA2	SDRDATA2	Hiz	Hiz
•			SDRDATA3	SDRDATA3	Hiz	Hiz
•			SDRDATA4	SDRDATA4	Hiz	Hiz
•			SDRDATA5	SDRDATA5	Hiz	Hiz
•			SDRDATA6	SDRDATA6	Hiz	Hiz
•			SDRDATA7	SDRDATA7	Hiz	Hiz
•			SDRDATA8	SDRDATA8	Hiz	Hiz
•			SDRDATA9	SDRDATA9	Hiz	Hiz
•			SDRDQM0	SDRDQM0	High	High
•			SDRDQM1	SDRDQM1	High	High
•			SDRRAS	SDRRAS	High	High
•			SDRWE	SDRWE	High	High
•	•	•	SWDCLK/ GPIO58/ EXTINT58/ DMCKO1	SWDCLK	Hiz	Hiz
•	•	•	SWDIO/ GPIO59/ EXTINT59/ DMDIN1	SWDIO	Hiz	Hiz
•	•	•	NRES	NRES	Hiz	Hiz
•	•	•	TEST	TEST	Hiz	Hiz
•		•	XTALINFO0	XTALINFO0	Hiz	Hiz
•		•	XTALINFO1	XTALINFO1	Hiz	Hiz
•	•	•	BMODE0	BMODE0	Hiz	Hiz
•	•	•	BMODE1	BMODE1	Hiz	Hiz
•		•	RTCMODE	RTCMODE	Hiz	Hiz
•		•	KEYINT0	KEYINT0	PD	PD
•		•	KEYINT1	KEYINT1	PD	PD
•		•	KEYINT2	KEYINT2	PD	PD
•	•	•	BACKUPB	BACKUPB	Hiz	Hiz
•	•	•	RTCINT	RTCINT	(Not Determined)	(Not Determined)
•	•	•	VDET	VDET	Hiz	Hiz
•	•	•	LOUT/ GPLOUT	LOUT	Hiz	Hiz
•	•	•	ROUT/ GPROUT	ROUT	Hiz	Hiz

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Table 7. PORT STATE TABLE (continued)

XBGA240	TQFP128L	WLP154	PIN NAME	Default Function (NRES=Low) (Note 22)	Port Status NRES=Low(i) (Note 23)	Port Status NRES=High(ii) (Note 23)
•	•	•	USBDM	USBDM	Hiz	Hiz
•	•	•	USBDP	USBDP	Hiz	Hiz
•	•	•	USBEXT12	USBEXT12	(Not Applicable)	(Not Applicable)
•	•	•	VCNT1	VCNT1	(Not Applicable)	(Not Applicable)
•	•	•	VCNT2	VCNT2	(Not Applicable)	(Not Applicable)
• (Note 27)	• (Note 27)	•	VCNT3	VCNT3	(Not Applicable)	(Not Applicable)
•	•	•	AN0	AN0	(Not Applicable)	(Not Applicable)
•	•	•	AN1	AN1	(Not Applicable)	(Not Applicable)
•	•	•	AN2	AN2	(Not Applicable)	(Not Applicable)
•	•	•	AN3	AN3	(Not Applicable)	(Not Applicable)
•	•	•	AN4	AN4	(Not Applicable)	(Not Applicable)
•	•	•	AN5	AN5	(Not Applicable)	(Not Applicable)
•			VR	VR	(Not Applicable)	(Not Applicable)
•			VRH	VRH	(Not Applicable)	(Not Applicable)
•			VRL	VRL	(Not Applicable)	(Not Applicable)
•	•	•	XIN1	XIN1	(Not Applicable)	(Not Applicable)
•	•	•	XIN32K	XIN32K	(Not Applicable)	(Not Applicable)
•	•	•	XOUT1	XOUT1	(Not Applicable)	(Not Applicable)
•	•	•	XOUT32K	XOUT32K	(Not Applicable)	(Not Applicable)

21. Means a port is available for each package. "PD" means pull down

22. Default function is port function set by NRES = Low

23. NRES = High (ii) occurs just after NRES = Low(i)

24. This port is set to output port and PU is disabled to be used as QSCS for SPI I/F chip select during serial flash boot mode.

25. This port is set to output port to be used as external power control during Internal ROM boot.

26. This port is set to output port to be used as boot monitor port during Internal ROM boot.

27. One of VCNT2 or VCNT3 is available

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电气规格

除非另有说明，“电气特性”表格中列出的是所列测试条件下的产品性能参数。如果在不同条件下运行，

产品性能可能与“电气特性”表格中所列性能参数不一致。

Table 8. MAXIMUM RATINGS (*V_{SS}* = 0 V)

Item	Symbol	Condition	Ratings	Unit
Maximum Power Supply Voltage	Vdd1 VddRTC VddXT1 AVddUSBPHY1 DvddUSBPHY1 AvddPLL1 AVddPLL2		-0.5 to 1.8	V
	AvddDAMPL AVddDAMPR		-0.5 to 2.5	V
	Vdd2 VddSD0 VddSD1 VddSD2 VddQSPI AvddPLL3 AvddADC AVddUSBPHY2		-0.5 to 4.6	V
Input Voltage	V _I		-0.5 to *Vdd* + 0.5	V
	V _{IUSB}	USBDP, USBDM Terminal	-0.5 to AVddUSBPHY2 + 0.5 (< 4.6)	V
Operating Ambient Temperature	Topr		-20 to +65	°C
Ambient Temperature of Preservation	Tstg		-55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

(参考譯文)

如果电压超过最大额定值表中列出的值范围，器件可能会损坏。如果超过任何这些限值，将无法保证器件功能，可能会导致器件损坏，影响可靠性。

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Table 9. RECOMMENDED OPERATING CONDITIONS (Ta = -20°C to +65°C)

Item	Symbol	Condition	Low Voltage Operation (Note 28)			High Voltage Operation (Note 28)			Unit	
			Min	Typ	Max	Min	Typ	Max		
Power Supply Voltage	Vdd1		0.93	1.0	1.27	1.1	1.2	1.27	V	
	VddXT1	(Note 29)	0.93	1.0	1.3	0.93	1.2	1.3	V	
	AVddPLL1		0.93	1.0	1.3	1.1	1.2	1.3	V	
	AVddPLL2		0.9	1.0	1.3	0.9	1.2	1.3	V	
	AVddPLL3		2.7	3.3	3.6	Same as left			V	
	VddRTC		0.9	1.0	1.1	Same as left			V	
	Vdd2			2.7	3.3	3.6	Same as left			V
				1.7	1.8	1.95	Same as left			V
	VddSD0			2.7	3.3	3.6	Same as left			V
				1.7	1.8	1.95	Same as left			V
	VddSD1			2.7	3.3	3.6	Same as left			V
				1.7	1.8	1.95	Same as left			V
	VddSD2			2.7	3.3	3.6	Same as left			V
				1.7	1.8	1.95	Same as left			V
	VddQSPI			2.7	3.3	3.6	Same as left			V
				1.7	1.8	1.95	Same as left			V
	AVddADC		2.7	3.3	3.6	Same as left			V	
	AVddUSBPHY1		(Note 30)	0.93	1.2	1.3	Same as left			V
			(Note 31)	1.08	1.2	1.3	Same as left			V
	DVddUSBPHY1		(Note 35)	0.93	1.2	1.3	Same as left			V
			(Note 31)	1.08	1.2	1.3	Same as left			V
	AVddUSBPHY2		(Note 30)	2.7	3.3	3.6	Same as left			V
			(Note 31)	3.0	3.3	3.6	Same as left			V
	AVddDAMPL			0.93	1.2	1.65	Same as left			V
		(Note 32)	0.93	1.2	1.95	Same as left			V	
AVddDAMPR			0.93	1.2	1.65	Same as left			V	
		(Note 32)	0.93	1.2	1.95	Same as left			V	
Input Range	VIN		0		*Vdd*	Same as left			V	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

推薦的工作範圍：

高于推荐工作范围表格中所列电压时，不保证能够正常运行。长时间在推荐工作范围表格中规定范围以外的电压下运行，可能会影响器件的可靠性。

28. Follow the operating frequency specifications because the operating frequency ranges are specified according to the operating voltage ranges.

29. Regarding Xtal frequency range, refer to the detailed datasheet.

30. While USB is not used.

31. While USB is used (including USB suspend mode).

32. While used as GPO (general purpose output) the output of which can be controlled by registers.

33. Power domains of Vdd1, AVddUSBPHY1 = DVddUSBPHY1, AVddPLL1, AVddPLL2, AVddPLL3, VddXT1 are divided, and different voltage can be supplied.

Power domains of Vdd2, VddSD0, VddSD1, VddSD2, VddQSPI, AVddADC, AVddUSBPHY2, AVddPLL3, AvddDAMPL = AVddDAMPR are divided, and difference voltage can be supplied.

If power is supplied to one of the power supply pins above, all of other power supply pins should be supplied.

VddRTC can be supplied if BACKUPB is set to low, while other power supply pins are not supplied.

Table 10. RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Function	Low Voltage Operation			High Voltage Operation		Unit
Xtal Input Frequency	Fxin1	System, Audio clock (XT1 oscillator)	12 MHz or 20 MHz tolerance : ± 200 ppm or less Jitter : ± 50 ps or less (Note 37)			12 MHz or 20 MHz or 24 MHz or 48 MHz tolerance : ± 200 ppm or less Jitter : ± 50 ps or less (Note 37)		-
	FxinRTC	RTC clock (XTRTC oscillator)	32.768 kHz Jitter : ± 500 ps or less			Same as left		-
	Frc	RC (RC oscillator)	0.4 (Note 38)	1 (Note 38)	2 (Note 38)	Same as left		MHz
Time for Xtal Stable	Txin1				3 (Note 40)	Same as left		ms
	TxinRTC				1000 (Note 40)	Same as left		ms
Internal Clock Frequency	Farm	Cortex-M3	0		100	0	160 (Note 39)	MHz
	Fahb	AHB	0		100	0	160 (Note 39)	MHz
	Fapb	APB	0		100	0	160 (Note 39)	MHz
	Fdsp	DSP	0		100	0	160 (Note 39)	MHz
	Faud (Note 34)	AUDCLK(768fs)	0	33.8688	147.456	Same as left		MHz
	Fdec	DECCLK(Note 35) (MP3 Decoder)	0	16.9344	73.728	Same as left		MHz
	Fenc	ENCCLK(Note 36) (MP3 Encoder)	0	8.4672	36.864	Same as left		MHz

34. Audio blocks run on $256 * F_s$ (sampling frequency) clock.

However, Class-D AMP, etc run on $384 * F_s$ (sampling frequency).

These clocks are generated from $768 * F_s$ (Base Clock) divided by 3 and 2 respectively.

35. MP3 Decoder runs on clock of $384 * F_s$ (sampling frequency of MPEG1 mode).

It runs on the clock of the same frequency as MPEG1 mode during MPEG2 / 2.5 mode. For example, even when operating in MPEG2 / 2.5 mode ($F_s = 22.05 / 11.025$ KHz as an example), please supplies 16.9344 MHz (= $384 * 44.1$ kHz) clock which is the same clock frequency as MPEG1 mode.

36. MP3 Encoder runs on clock of $192 * F_s$ (sampling frequency of MPEG1 mode).

It runs on the clock of the same frequency as MPEG1 mode during MPEG2 / 2.5 mode. For example, even when operating in MPEG2 / 2.5 mode ($F_s = 22.05 / 11.025$ KHz as an example), please supplies 8.4672 Mhz (= $192 * 44.1$ kHz) clock which is the same clock frequency as MPEG1 mode.

37. Refer to the detailed datasheet. If USB function is not used, the specification required may be relaxed. Please contact our representative in detail.

38. $V_{dd1} = 0.93$ V to 1.27 V, $T_a = -20^\circ\text{C}$ to 65°C .

39. When Farm, Fdsp are over 100 MHz, 1 * Wait is required for Cortex-M3 and LPDSP32 to access internal ROM by the register described in the ProgrammersModel_SystemController as memory access control register4.

40. These are just reference values under $T_a = 25^\circ\text{C}$, and need to be adjusted to customer board situation.

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Table 11. DC CHARACTERISTICS

(Vdd2= 2.7 V to 3.6V, VddRTC = 0.9 V to 1.1 V, VddSD0 = 2.7 V to 3.6 V, VddSD1 = 2.7 V to 3.6V, VddSD2 = 2.7 V to 3.6 V, VddQSPI = 2.7 V to 3.6 V, Ta = -20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Input H Voltage	V _{IH}	(1)	CMOS	0.7 × Vdd2			V
		(2)		0.7 × VddSD0			V
		(3)		0.7 × VddSD1			V
		(4)		0.7 × VddSD2			V
		(5)	Schmitt	0.75 × Vdd2			V
		(21)		0.75 × VddSD1			V
		(6)		0.75 × VddSD2			V
		(7)		0.75 × VddQSPI			V
		(8)	CMOS	0.7 × VddRTC			V
		(9)	Schmitt	0.7 × VddRTC			V
Input L Voltage	V _{IL}	(1)	CMOS			0.3 × Vdd2	V
		(2)				0.3 × VddSD0	V
		(3)				0.3 × VddSD1	V
		(4)				0.3 × VddSD2	V
		(5)	Schmitt			0.25 × Vdd2	V
		(21)				0.25 × VddSD1	V
		(6)				0.25 × VddSD2	V
		(7)				0.25 × VddQSPI	V
		(8)	CMOS			0.2 × VddRTC	V
		(9)	Schmitt			0.2 × VddRTC	V

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Table 11. DC CHARACTERISTICS (continued)

(Vdd2= 2.7 V to 3.6V, VddRTC = 0.9 V to 1.1 V, VddSD0 = 2.7 V to 3.6 V, VddSD1 = 2.7 V to 3.6V, VddSD2 = 2.7 V to 3.6 V, VddQSPI = 2.7 V to 3.6 V, Ta = -20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Output H Voltage	V _{OH}	(10)(12)	I _{OH} = -1 mA	Vdd2 - 0.4			V
		(11)		VddQSPI - 0.4			V
		(10)(13)(14)	I _{OH} = -2 mA	Vdd2 - 0.4			V
		(11)		VddQSPI - 0.4			V
		(15)		VddSD1 - 0.4			V
		(12)		VddSD2 - 0.4			V
		(10)(13)	I _{OH} = -4 mA	Vdd2 - 0.4			V
		(11)		VddQSPI - 0.4			V
		(12)		VddSD2 - 0.4			V
		(16)	I _{OH} = -6 mA	VddQSPI - 0.4			V
		(17)		VddSD0 - 0.4			V
		(18)		VddSD1 - 0.4			V
		(19)		VddSD2 - 0.4			V
		(13)	I _{OH} = -8 mA	Vdd2 - 0.4			V
		(16)		VddQSPI - 0.4			V
		(17)		VddSD0 - 0.4			V
		(18)		VddSD1 - 0.4			V
		(19)		VddSD2 - 0.4			V
		(16)	I _{OH} = -10 mA	VddQSP - 0.4			V
		(17)		VddSD0 - 0.4			V
(18)	VddSD1 - 0.4				V		
(19)	VddSD2 - 0.4				V		

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Table 11. DC CHARACTERISTICS (continued)

(Vdd2= 2.7 V to 3.6V, VddRTC = 0.9 V to 1.1 V, VddSD0 = 2.7 V to 3.6 V, VddSD1 = 2.7 V to 3.6V, VddSD2 = 2.7 V to 3.6 V, VddQSPI = 2.7 V to 3.6 V, Ta = -20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Output L Voltage	V _{OL}	(10)(12)	I _{OL} = 1 mA			0.4	V
		(11)				0.4	V
		(10)(13)(14)	I _{OL} = 2 mA			0.4	V
		(11)				0.4	V
		(15)				0.4	V
		(12)	I _{OL} = 4 mA			0.4	V
		(10)(13)				0.4	V
		(11)				0.4	V
		(16)	I _{OL} = 6 mA			0.4	V
		(17)				0.4	V
		(18)				0.4	V
		(19)				0.4	V
		(13)	I _{OL} = 8 mA			0.4	V
		(16)				0.4	V
		(17)				0.4	V
		(18)				0.4	V
		(19)	I _{OL} = 10 mA			0.4	V
		(16)				0.4	V
		(17)				0.4	V
		(18)				0.4	V
(19)	I _{OL} = 0.3 mA			0.4	V		
(20)				0.4	V		
(16)				0.4	V		
(17)				0.4	V		
Pull-up Resister	R _{up}	(28)		25		75	kΩ
		(29)		10		100	kΩ
		(30)		18		50	kΩ
Pull-down Resister	R _{dn}	(25)		25		75	kΩ
		(26)		10		100	kΩ
		(27)		10		100	kΩ
Input Leak Current	I _{IL}	(1)(2)(3)(4) (5)(6)(7)(8) (9)(21)	V _I = V _{dd} * = V _{ss}	-10		10	μA
Output Leak Current	I _{OZ}	(10)(11)(12)(13) (14)(15)(16)(17) (18)(19)	HiZ output	-10		10	μA
		(23)(24)		-10		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

(参考譯文)

除非另有说明，“电气特性”表格中列出的是所列测试条件下的产品性能参数。如果在不同条件下运行，产品性能可能与“电气特性”表格中所列性能参数不一致。

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Table 12. DC CHARACTERISTICS

(Vdd2 = 1.7 V to 1.95 V, VddSD0 = 1.7 V to 1.95 V, VddSD1 = 1.7 V to 1.95 V, VddSD2 = 1.7 V to 1.95 V, VddQSPI = 1.7 V to 1.95 V, AVddDAMPL = 0.93 V to 1.95 V, AVddDAMPR = 0.93 V to 1.95 V, Ta = -20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Input H Voltage	V _{IH}	(1)	CMOS	0.7 × Vdd2			V
		(2)		0.7 × VddSD0			V
		(3)		0.7 × VddSD1			V
		(4)		0.7 × VddSD2			V
		(5)	Schmitt	0.75 × Vdd2			V
		(21)		0.75 × VddSD1			V
		(6)		0.75 × VddSD2			V
		(7)		0.75 × VddQSPI			V
Input L Voltage	V _{IL}	(1)	CMOS			0.3 × Vdd2	V
		(2)				0.3 × VddSD0	V
		(3)				0.3 × VddSD1	V
		(4)				0.3 × VddSD2	V
		(5)	Schmitt			0.25 × Vdd2	V
		(21)				0.25 × VddSD1	V
		(6)				0.25 × VddSD2	V
		(7)				0.25 × VddQSPI	V

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Table 12. DC CHARACTERISTICS (continued)

(Vdd2 = 1.7 V to 1.95 V, VddSD0 = 1.7 V to 1.95 V, VddSD1 = 1.7 V to 1.95 V, VddSD2 = 1.7 V to 1.95 V, VddQSPI = 1.7 V to 1.95 V, AVddDAMPL = 0.93 V to 1.95 V, AVddDAMPR = 0.93 V to 1.95 V, Ta = -20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Output H Voltage	V _{OH}	(10)(12)	I _{OH} = -0.5 mA	Vdd2 - 0.4			V
		(11)		VddQSPI - 0.4			V
		(10)(13)(14)	I _{OH} = -1 mA	Vdd2 - 0.4			V
		(11)		VddQSPI - 0.4			V
		(15)		VddSD1 - 0.4			V
		(12)		VddSD2 - 0.4			V
		(10)(13)	I _{OH} = -2 mA	Vdd2 - 0.4			V
		(11)		VddQSPI - 0.4			V
		(12)		VddSD2 - 0.4			V
		(16)	I _{OH} = -3 mA	VddQSPI - 0.4			V
		(17)		VddSD0 - 0.4			V
		(18)		VddSD1 - 0.4			V
		(19)		VddSD2 - 0.4			V
		(13)	I _{OH} = -4 mA	Vdd2 - 0.4			V
		(16)		VddQSPI - 0.4			V
		(17)		VddSD0 - 0.4			V
		(18)		VddSD1 - 0.4			V
		(19)		VddSD2 - 0.4			V
		(23)	I _{OH} = -8 mA (Note 46)	AvddDAMPL - 0.4			V
		(24)	I _{OH} = -8 mA (Note 46)	AvddDAMPR - 0.4			V
		(16)	I _{OH} = -5 mA	VddQSPI - 0.4			V
		(17)		VddSD0 - 0.4			V
		(18)		VddSD1 - 0.4			V
		(19)		VddSD2 - 0.4			V

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Table 12. DC CHARACTERISTICS (continued)

(Vdd2 = 1.7 V to 1.95 V, VddSD0 = 1.7 V to 1.95 V, VddSD1 = 1.7 V to 1.95 V, VddSD2 = 1.7 V to 1.95 V, VddQSPI = 1.7 V to 1.95 V, AVddDAMPL = 0.93 V to 1.95 V, AVddDAMPR = 0.93 V to 1.95 V, Ta = -20°C to +65°C)

Item	Symbol	Pin	Condition	Min	Typ	Max	Unit
Output L Voltage	V _{OL}	(10)(11)(12)	I _{OL} = 0.5 mA			0.4	V
		(10)(13)(14)	I _{OL} = 1 mA			0.4	V
		(11)				0.4	V
		(15)				0.4	V
		(12)				0.4	V
		(10)(13)	I _{OL} = 2 mA			0.4	V
		(11)				0.4	V
		(12)				0.4	V
		(16)	I _{OL} = 3 mA			0.4	V
		(17)				0.4	V
		(18)				0.4	V
		(19)				0.4	V
		(13)	I _{OL} = 4 mA			0.4	V
		(16)				0.4	V
		(17)				0.4	V
		(18)				0.4	V
		(19)				0.4	V
		(23)	I _{OL} = 8 mA (Note 41)			0.4	V
		(24)	I _{OL} = 8 mA (Note 41)			0.4	V
		(16)	I _{OL} = 5 mA			0.4	V
(17)				0.4	V		
(18)				0.4	V		
(19)				0.4	V		
Pull-up Resistor	R _{up}	(28)		25		75	kΩ
		(29)		30		200	kΩ
		(30)		18		50	kΩ
Pull-down Resistor	R _{dn}	(25)		25		75	kΩ
		(26)		30		200	kΩ
Input Leak Current	I _{IL}	(1)(2)(3)(4) (5)(6)(7)(8) (9)(21)	V _I = V _{dd} * = V _{ss}	-10		10	μA
Output Leak Current	I _{oz}	(10)(11)(12)(13) (14)(15)(16)(17) (18)(19)	HiZ output	-10		10	μA
		(23)(24)		-10		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

(参考譯文)

除非另有说明，“电气特性”表格中列出的是所列测试条件下的产品性能参数。如果在不同条件下运行，产品性能可能与“电气特性”表格中所列性能参数不一致。

41. Set DAMPCTL register as below.

- DZCTL: DSLEEP=1. (don't care DSL value)

- G DZINP: DZINP14=1, other DZINPx=0

This DC characteristics can be applied while Class-D AMP used as GPO.

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- (1) SDRDATA15, SDRDATA14, SDRDATA13, SDRDATA12, SDRDATA11, SDRDATA10, SDRDATA9, SDRDATA8, SDRDATA7, SDRDATA6, SDRDATA5, SDRDATA4, SDRDATA3, SDRDATA2, SDRDATA1, SDRDATA0
- (2) SDCMD0, SDAT03, SDAT02, SDAT01, SDAT00
- (3) SDCLK1(GPIO22), SDCMD1(GPIO23), SDAT10(GPIO24), SDAT11(GPIO25), SDAT12(GPIO26), SDAT13(GPIO27)
- (4) TXD1(GPIO04), RXD1(GPIO05), TIOCA00(GPIO09), TIOCA01(GPIO0A), CTS1(GPIO56), RTS1(GPIO57)
- (5) TEST, NRES, BMODE1, BMODE0, TCLKA0(GPIO00), TCLKB0(GPIO01), TIOCB00(GPIO02), NCS0(GPIO06), SCL0(GPIO07), SDA0(GPIO08), NCS1(GPIO10), BCK1(GPIO13), LRCK1(GPIO14), DOUT1(GPIO15), NLBEXA0(GPIO16), NRD(GPIO17), MCLK0(GPIO18), BCK0(GPIO19), LRCK0(GPIO1A), DIN0(GPIO1B), DOUT0(GPIO1C), SCK0(GPIO1D), SDI0(GPIO1E), SDO0(GPIO1F), SDRADDR12(GPIO2A), SCL1(GPIO2B), SDA1(GPIO2C), SDRADDR11(GPIO2D), EXTINT2E(GPIO2E), EXTINT2F(GPIO2F), NWRENWRL(GPIO30), NHBNWRH(GPIO31), EXA1(GPIO32), EXA2(GPIO33), EXA3(GPIO34), EXA4(GPIO35), EXA5(GPIO36), EXA6(GPIO37), EXA7(GPIO38), EXA8(GPIO39), EXA9(GPIO3A), EXA10(GPIO3B), EXA11(GPIO3C), EXA12(GPIO3D), EXA13(GPIO3E), EXA14(GPIO3F), EXA15(GPIO40), EXA16(GPIO41), EXA17(GPIO42), EXA18(GPIO43), EXA19(GPIO44), EXA20(GPIO45), EXD0(GPIO46), EXD1(GPIO47), EXD2(GPIO48), EXD3(GPIO49), EXD4(GPIO4A), EXD5(GPIO4B), EXD6(GPIO4C), EXD7(GPIO4D), EXD8(GPIO4E), EXD9(GPIO4F), EXD10(GPIO50), EXD11(GPIO51), EXD12(GPIO52), EXD13(GPIO53), EXD14(GPIO54), EXD15(GPIO55), SWDCLK(GPIO58), SWDIO(GPIO59), XTALINFO1, XTALINFO0
- (6) TIOCA00(GPIO09), TMS(GPIO28), TCK(GPIO29)
- (7) SCK1(GPIO0D), SDI1(GPIO0E), SDO1(GPIO0F), SWP1(GPIO11), SHOLD1(GPIO12), TIOCB01(GPIO03), TXD2(GPIO0B), RXD2(GPIO0C)
- (8) VDET, RTCMODE
- (9) BACKUPB, KEYINT2, KEYINT1, KEYINT0
- (10) TCLKA0(GPIO00), TCLKB0(GPIO01), TIOCB00(GPIO02), SCL0(GPIO07), SDA0(GPIO08), BCK1(GPIO13), LRCK1(GPIO14), DOUT1(GPIO15), MCLK0(GPIO18), BCK0(GPIO19), LRCK0(GPIO1A), DIN0(GPIO1B), DOUT0(GPIO1C), SCK0(GPIO1D), SDI0(GPIO1E), SDO0(GPIO1F), SCL1(GPIO2B), SDA1(GPIO2C), EXTINT2E(GPIO2E), EXTINT2F(GPIO2F), SWDCLK(GPIO58)
- (11) TXD2(GPIO0B), RXD2(GPIO0C)
- (12) TMS(GPIO28), TCK(GPIO29)
- (13) SDRWE, SDRRAS, SDRDQM1, SDRDQM0, SDRDATA9, SDRDATA8, SDRDATA7, SDRDATA6, SDRDATA5, SDRDATA4, SDRDATA3, SDRDATA2, SDRDATA15, SDRDATA14, SDRDATA13, SDRDATA12, SDRDATA11, SDRDATA10, SDRDATA9, SDRDATA8, SDRDATA7, SDRDATA6, SDRDATA5, SDRDATA4, SDRDATA3, SDRDATA2, SDRDATA1, SDRDATA0, SDRCS, SDRCLK, SDRCKE, SDRCAS, SDRBA1, SDRBA0, SDRADDR9, SDRADDR8, SDRADDR7, SDRADDR6, SDRADDR5, SDRADDR4, SDRADDR3, SDRADDR2, SDRADDR1, SDRADDR0, NCS0(GPIO06), NCS1(GPIO10), NLBEXA0(GPIO16), NRD(GPIO17), SDRADDR12(GPIO2A), SDRADDR11(GPIO2D), NWRENWRL(GPIO30), NHBNWRH(GPIO31), EXA1(GPIO32), EXA2(GPIO33), EXA3(GPIO34), EXA4(GPIO35), EXA5(GPIO36), EXA6(GPIO37), EXA7(GPIO38), EXA8(GPIO39), EXA9(GPIO3A), EXA10(GPIO3B), EXA11(GPIO3C), EXA12(GPIO3D), EXA13(GPIO3E), EXA14(GPIO3F), EXA15(GPIO40), EXA16(GPIO41), EXA17(GPIO42), EXA18(GPIO43), EXA19(GPIO44), EXA20(GPIO45), EXD0(GPIO46), EXD1(GPIO47), EXD2(GPIO48), EXD3(GPIO49), EXD4(GPIO4A), EXD5(GPIO4B), EXD6(GPIO4C), EXD7(GPIO4D), EXD8(GPIO4E), EXD9(GPIO4F), EXD10(GPIO50), EXD11(GPIO51), EXD12(GPIO52), EXD13(GPIO53), EXD14(GPIO54), EXD15(GPIO55), XTALINFO1, XTALINFO0
- (14) BMODE1, BMODE0, SWDIO(GPIO59)
- (15) TDI(GPIO20), TDO(GPIO21)
- (16) TIOCB01(GPIO03), SCK1(GPIO0D), SDI1(GPIO0E), SDO1(GPIO0F), SWP1(GPIO11), SHOLD1(GPIO12)
- (17) SDCMD0, SDCLK0, SDAT03, SDAT02, SDAT01, SDAT00
- (18) SDCLK1(GPIO22), SDCMD1(GPIO23), SDAT10(GPIO24), SDAT11(GPIO25), SDAT12(GPIO26), SDAT13(GPIO27)
- (19) TXD1(GPIO04), RXD1(GPIO05), TIOCA00(GPIO09), TIOCA01(GPIO0A), CTS1(GPIO56), RTS1(GPIO57)
- (20) RTCINT
- (21) TDI(GPIO20), TDO(GPIO21)
- (22) LOUT(used as GPLOUT)
- (23) ROUT(used as GPROUT)
- (24) BMODE1, BMODE0
- (25) SDRDATA9, SDRDATA8, SDRDATA7, SDRDATA6, SDRDATA5, SDRDATA4, SDRDATA3, SDRDATA2, SDRDATA15, SDRDATA14, SDRDATA13, SDRDATA12, SDRDATA11, SDRDATA10, SDRDATA9, SDRDATA8, SDRDATA7, SDRDATA6, SDRDATA5, SDRDATA4, SDRDATA3, SDRDATA2, SDRDATA1, SDRDATA0, SDCMD0, SDAT03, SDAT02, SDAT01, SDAT00, TCLKA0(GPIO00), TCLKB0(GPIO01), TIOCB00(GPIO02), TIOCB01(GPIO03), TXD1(GPIO04), RXD1(GPIO05), SCL0(GPIO07), SDA0(GPIO08), TIOCA00(GPIO09), TIOCA01(GPIO0A), TXD2(GPIO0B), RXD2(GPIO0C), SCK1(GPIO0D), SDI1(QIO0)(GPIO0E), SDO1(QIO1)(GPIO0F), SWP1(QIO2)(GPIO11), SHOLD1(QIO3)(GPIO12), BCK1(GPIO13), LRCK1(GPIO14), DOUT1(GPIO15), NLBEXA0(GPIO16), NRD(GPIO17), MCLK0(GPIO18), BCK0(GPIO19), LRCK0(GPIO1A), DIN0(GPIO1B), DOUT0(GPIO1C), SCK0(GPIO1D), SDI0(GPIO1E), SDO0(GPIO1F), TDI(GPIO20), TDO(GPIO21), SDCLK1(GPIO22), SDCMD1(GPIO23), SDAT10(GPIO24), SDAT11(GPIO25), SDAT12(GPIO26), SDAT13(GPIO27), TMS(GPIO28), TCK(GPIO29), SDRADDR12(GPIO2A), SCL1(GPIO2B), SDA1(GPIO2C), SDRADDR11(GPIO2D), EXTINT2E(GPIO2E), EXTINT2F(GPIO2F), NWRENWRL(GPIO30), NHBNWRH(GPIO31), EXA1(GPIO32), EXA2(GPIO33), EXA3(GPIO34), EXA4(GPIO35), EXA5(GPIO36), EXA6(GPIO37), EXA7(GPIO38), EXA8(GPIO39), EXA9(GPIO3A), EXA10(GPIO3B), EXA11(GPIO3C), EXA12(GPIO3D), EXA13(GPIO3E), EXA14(GPIO3F), EXA15(GPIO40), EXA16(GPIO41), EXA17(GPIO42), EXA18(GPIO43), EXA19(GPIO44), EXA20(GPIO45), EXD0(GPIO46), EXD1(GPIO47), EXD2(GPIO48), EXD3(GPIO49), EXD4(GPIO4A), EXD5(GPIO4B), EXD6(GPIO4C), EXD7(GPIO4D), EXD8(GPIO4E), EXD9(GPIO4F), EXD10(GPIO50), EXD11(GPIO51), EXD12(GPIO52), EXD13(GPIO53), EXD14(GPIO54), EXD15(GPIO55), CTS1(GPIO56), RTS1(GPIO57), SWDCLK(GPIO58)
- (26) KEYINT2, KEYINT1, KEYINT0
- (27) SDCMD0, SDAT03, SDAT02, SDAT01, SDAT00, BMODE1, BMODE0, TXD1(GPIO04), RXD1(GPIO05), TIOCA00(GPIO09), TIOCA01(GPIO0A), SDCLK1(GPIO22), SDCMD1(GPIO23), SDAT10(GPIO24), SDAT11(GPIO25), SDAT12(GPIO26), SDAT13(GPIO27), CTS1(GPIO56), RTS1(GPIO57)
- (28) TCLKA0(GPIO00), TCLKB0(GPIO01), TIOCB00(GPIO02), TIOCB01(GPIO03), NCS0(GPIO06), SCL0(GPIO07), SDA0(GPIO08), TXD2(GPIO0B), RXD2(GPIO0C), SCK1(GPIO0D), SDI1(QIO0)(GPIO0E), SDO1(QIO1)(GPIO0F), NCS1(GPIO10), SWP1(QIO2)(GPIO11), SHOLD1(QIO3)(GPIO12), BCK1(GPIO13), LRCK1(GPIO14), DOUT1(GPIO15), MCLK0(GPIO18), BCK0(GPIO19), LRCK0(GPIO1A), DIN0(GPIO1B), DOUT0(GPIO1C), SCK0(GPIO1D), SDI0(GPIO1E), SDO0(GPIO1F), TDI(GPIO20), TDO(GPIO21), TMS(GPIO28), TCK(GPIO29), SDRADDR12(GPIO2A), SCL1(GPIO2B), SDA1(GPIO2C), SDRADDR11(GPIO2D), EXTINT2E(GPIO2E), EXTINT2F(GPIO2F), SWDCLK(GPIO58), SWDIO(GPIO59), XTALINFO1, XTALINFO0
- (29) SDCMD0, SDAT03, SDAT02, SDAT01, SDAT00
- (30) DC characteristics for these pins are not included: VR, VRH, VRL, USBDM, USBDP, USBEXT12, VCNT1, VCNT2, VCNT3, AN0, AN1, AN2, AN3, AN4, AN5, XIN1, XIN32K, XOUT1, XOUT32K, LOUT (Class-D AMP), ROUT (Class-D AMP)

LC823450

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing) [†]
LC823450TA-2H	TQFP128 14x14 / TQFP128L (Pb-Free / Halogen Free)	450 / Tray JEDEC
LC823450XATBG	WLCSP154, 5.52x5.33 (Pb-Free / Halogen Free)	1000 / Tape & Reel
LC823450XBTBG	WLCSP154, 5.52x5.33 (Pb-Free / Halogen Free)	1000 / Tape & Reel
LC823450XCTBG	WLCSP154, 5.52x5.33 (Pb-Free / Halogen Free)	1000 / Tape & Reel
LC823450XDTBG	WLCSP154, 5.52x5.33 (Pb-Free / Halogen Free)	1000 / Tape & Reel
LC823450RAH-xx (Under planning)	XBGA240 (Under planning)	Under planning

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

LC823450

应用框图

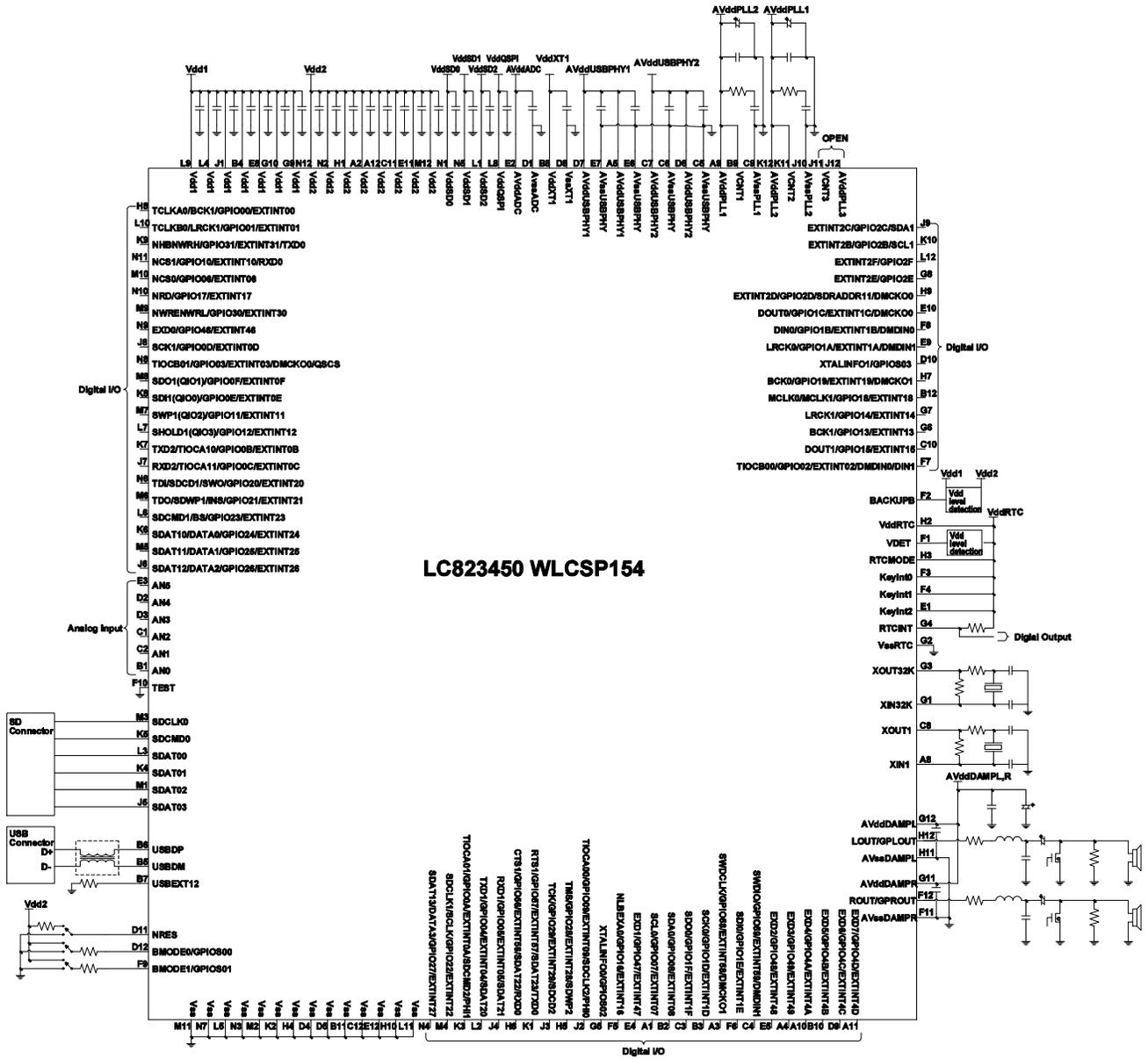
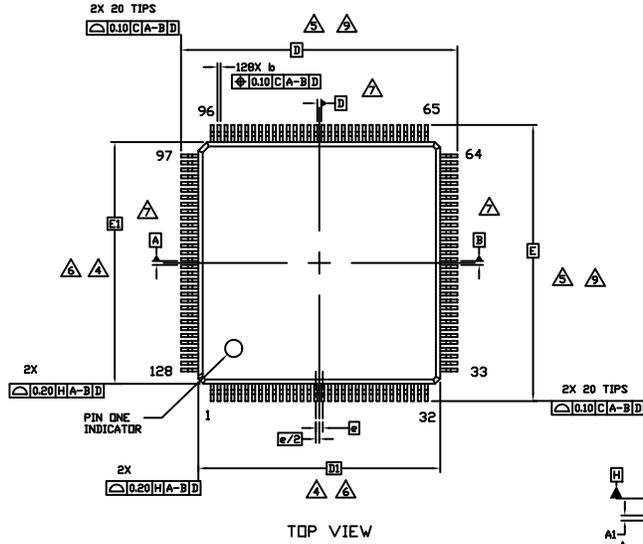


Figure 6. Application Diagram

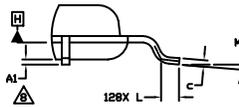
LC823450

PACKAGE DIMENSIONS

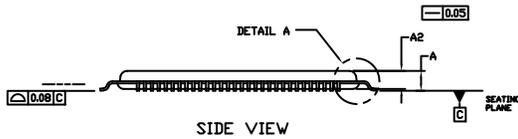
TQFP128 14x14 / TQFP128L
CASE 932BA
ISSUE A



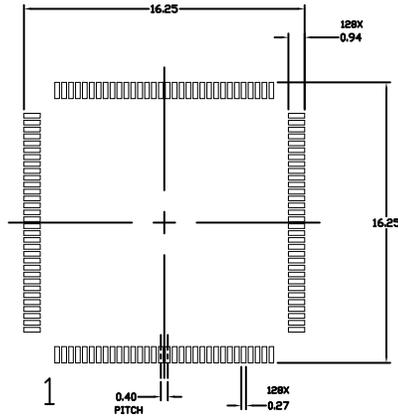
TOP VIEW



DETAIL A



SIDE VIEW



RECOMMENDED
MOUNTING FOOTPRINT

NOTES:

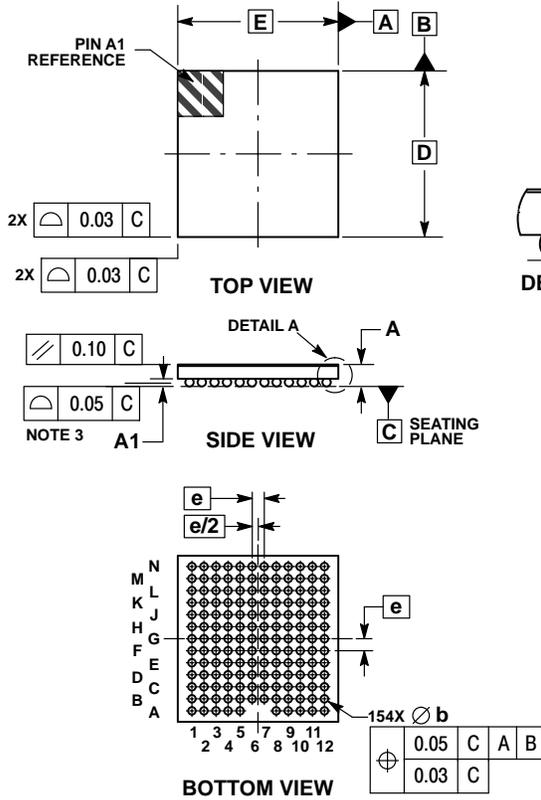
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
5. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15.
6. DIMENSIONS D1 AND E1 TO BE DETERMINED AT DATUM PLANE H.
7. DATUMS A-B AND D ARE DETERMINED AT DATUM PLANE H.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
9. DIMENSIONS D AND E TO BE DETERMINED AT DATUM PLANE C.

DIM	MILLIMETERS	
	MIN.	MAX.
A	---	1.20
A1	0.05	0.15
A2	1.00 REF	
b	0.13	0.23
c	0.09	0.20
D	16.00 BSC	
D1	14.00 BSC	
E	16.00 BSC	
E1	14.00 BSC	
e	0.40 BSC	
L	0.45	0.75
M	0°	7°

LC823450

PACKAGE DIMENSIONS

WLCSP154, 5.52x5.33
CASE 567LD
ISSUE A

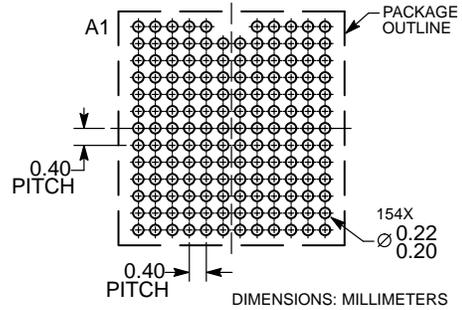


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.73
A1	0.18	0.24
A3	0.04 REF	
b	0.23	0.29
D	5.52 BSC	
E	5.33 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

* The diameter of footprint of the solder ball is as follows.

Table 13.

Package Code	Size of the Footprint
XA, XB	ϕ 0.20
XC, XD	ϕ 0.22

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